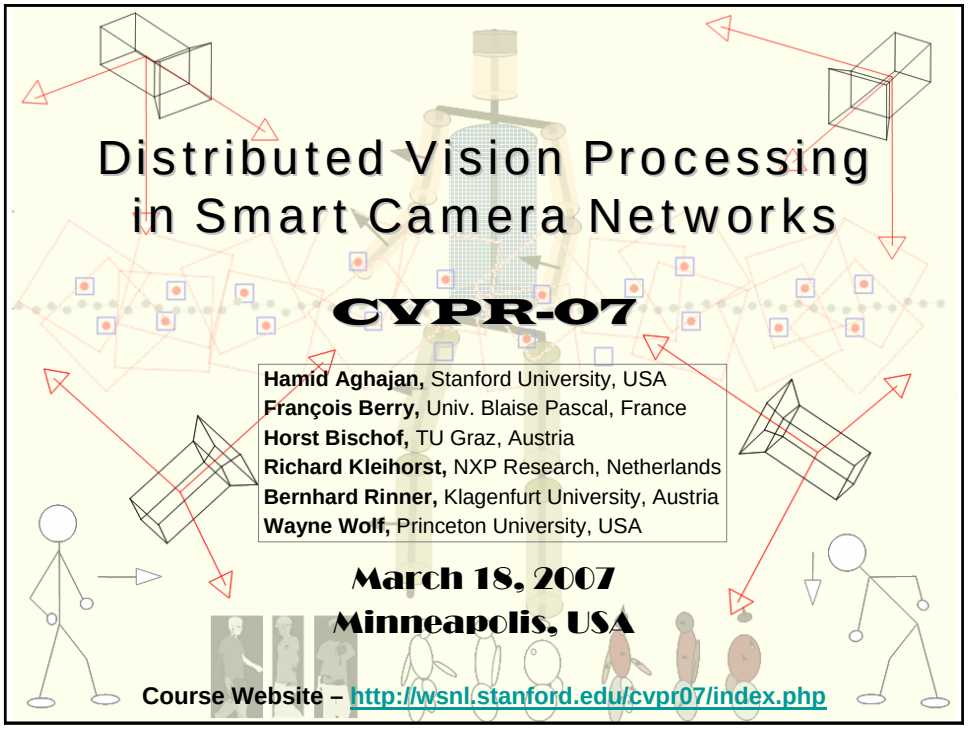
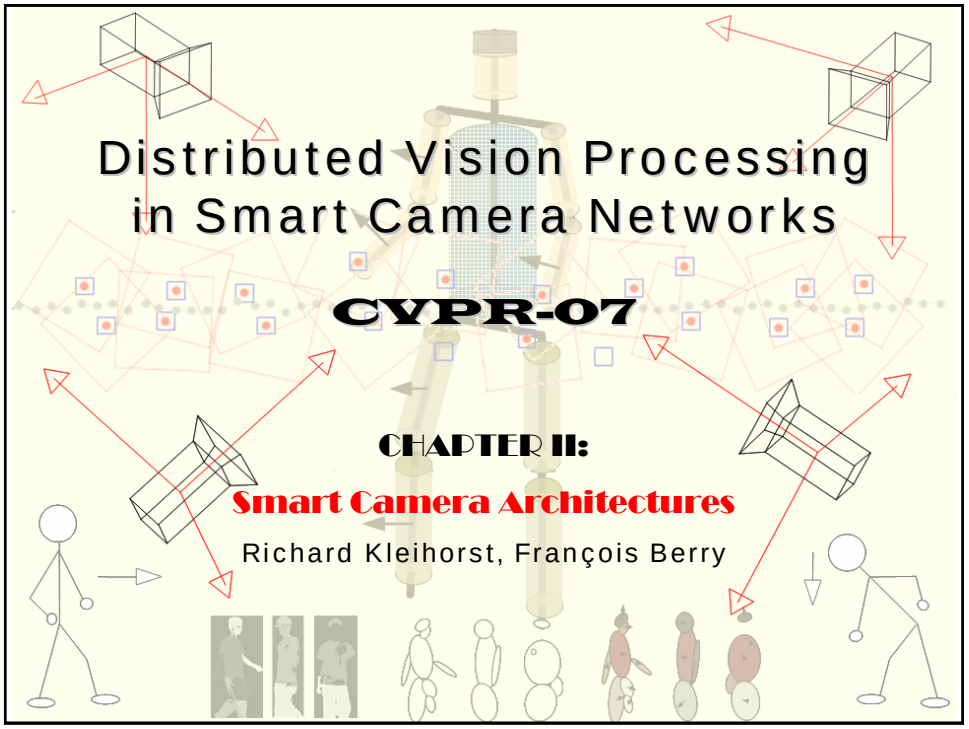


Outline



Smart Camera for Active Vision

Contact: François Berry
Francois.BERRY <AT> lasmea.univ-bpclermont.fr
LASMEA – CNRS

Active Vision and Smart Cameras

- Active vision processes imply continuous feedback between sensing devices and processing units
- In a smart camera:
  - Imaging device allows full random access and a high dynamic range
  - Processing unit allows high parallelization (for low level vision tasks) and a signal processing unit (iterative algorithms, optimization tasks, …)
  - Preferential links between sensors and the processing unit
  - A high speed link between the smart camera and the host computer / network

Example of Active Vision

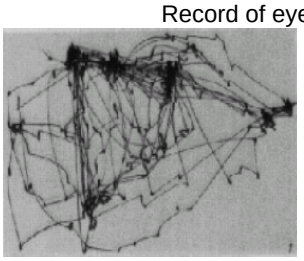
Yarbus, 1967

The activity of the eyes is related to the considered perception task

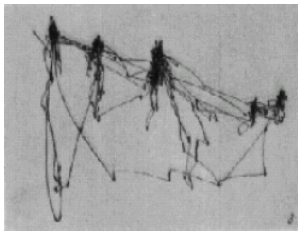
- The trajectories followed by the gaze depend on the task the observer has to perform
- The gaze tends to jump back and forth between the same parts of the scene
  - For example, the eyes and mouth in the picture of a face
- If the observers are asked specific questions about the images, their eyes would concentrate on areas of the image with relevance to the questions

Source Wikipedia

Record of eye movements



Free examination



"Give the ages of the persons"

SeeMos Project

- Primary objective:
  - A research platform dedicated to **active vision**
  - And in particular to the **early vision process**

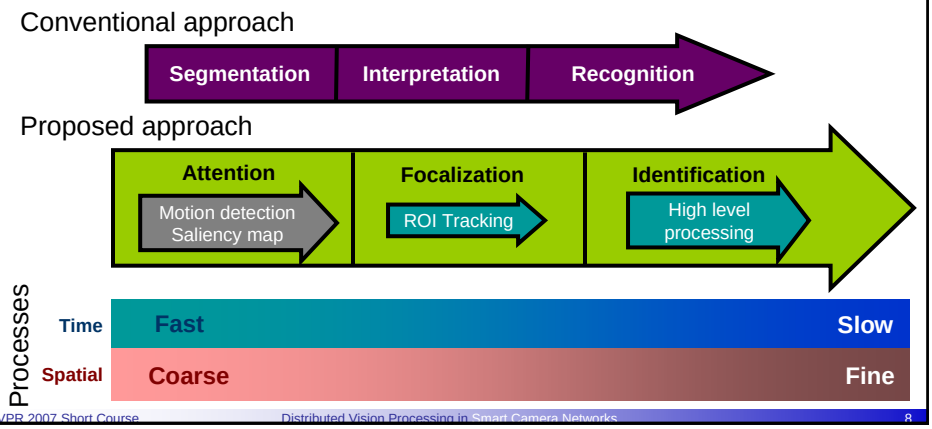
- Architecture based on:
  - FPGA
  - CMOS imager
  - Inertial devices
  - High speed communication
  - DSP-based co-designed board

http://wwwlasmea.univ-bpclermont.fr/Personnel/Francois.Berry/seemos.htm

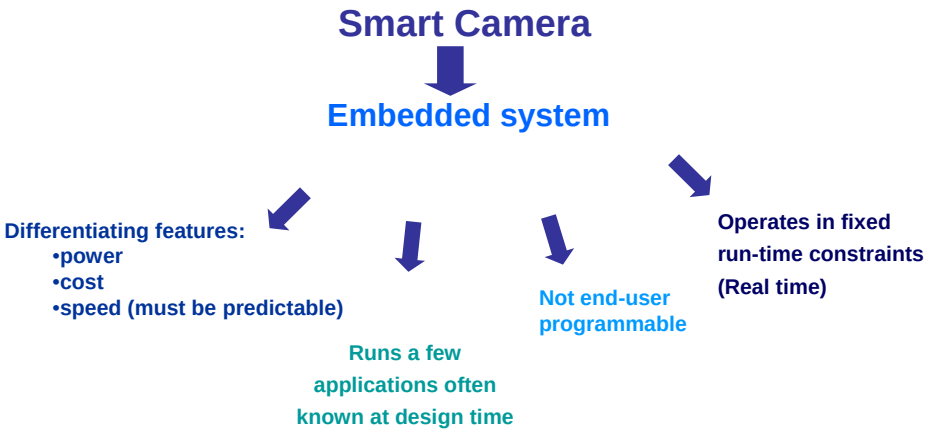
Motivation

"Active vision" vs. "Conventional vision"

- Active vision is an alternative approach to dealing with artificial vision problems
- The central idea, also known as the task-driven paradigm, is to take into account the perceptual aspect of visual tasks



Architecture



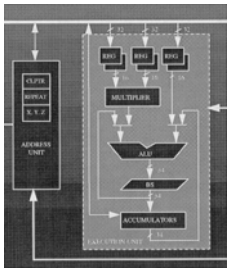
Processing Unit

Processor Approach

- **GPU and DSP**

DSP (Digital Signal Processor):

Microprocessor designed specifically for digital signal processing, generally in real-time computing



Features:

- Highly parallel accumulator and multiplier : MAC Operation
- Fixed-point arithmetic is often used to speed up arithmetic processing.

The DSPs supports 4 algorithms:

- Infinite Impulse Response (IIR) filters
- Finite Impulse Response (FIR) filters
- FFT
- Convolvers

TEXAS INSTRUMENTS ANALOG DEVICES

Processor Approach

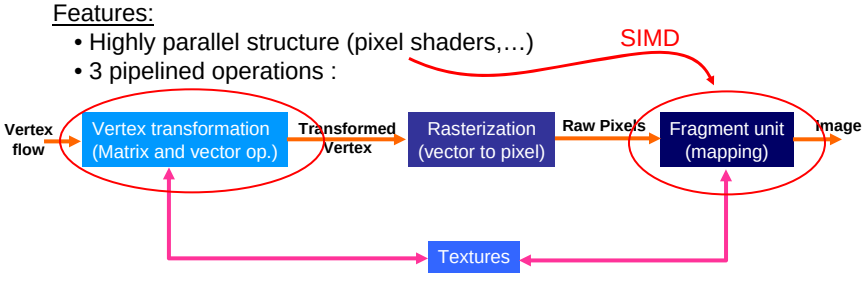
- **GPU and DSP**

GPU (Graphics Processing Unit):

Microprocessor dedicated to rendering and manipulating graphics

Features:

- Highly parallel structure (pixel shaders,…)
- 3 pipelined operations :



http://developer.nvidia.com/page/tools.html

NVIDIA ATI

Processing Unit

Technology

Processor approach:
DSP,
Media Processor,
GPU

Programmable Logic approach:
CPLD, FPGA

Programmable Logic Approach

- **FPGA (Field Programmable Gate Array):**
  It is an electronic component used to build dedicated digital cir

Integrated circuit able to change interconnectivity of a large number of fundamental computing components via configuration information stored in on-board static RAM

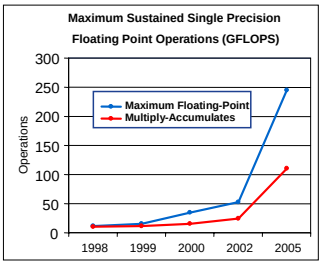
FPGA + Hardware Description (VHDL, Verilog) = Customized IC

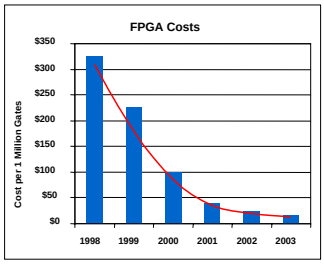
Customized IC
- Processor
- Specific glue logic
- Specific applications

ALTERA XILINX Actel Lattice Semiconductor Corporation

Programmable Logic Approach

- **FPGA (Field Programmable Gate Array):**
  - Increased speed & density
  - Increased I/O pin count and bandwidth
  - Lower power
  - Integration of hard IP (e.g. multipliers, processor soft cores,…)



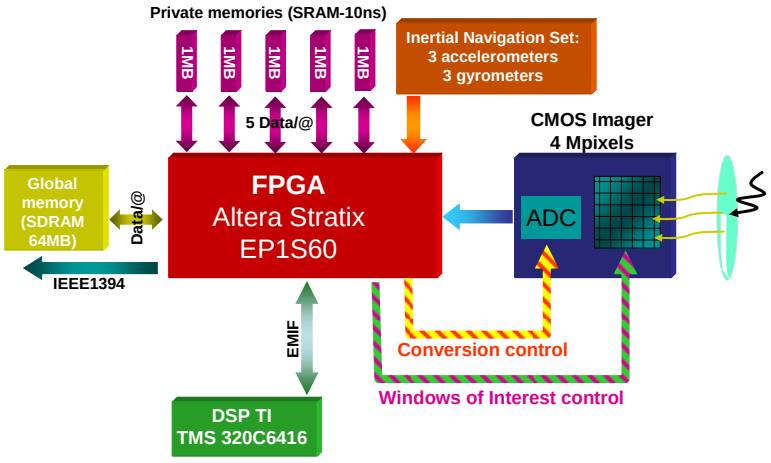


ALTERA. XILINX® Actel Lattice Semiconductor Corporation

Processing Unit

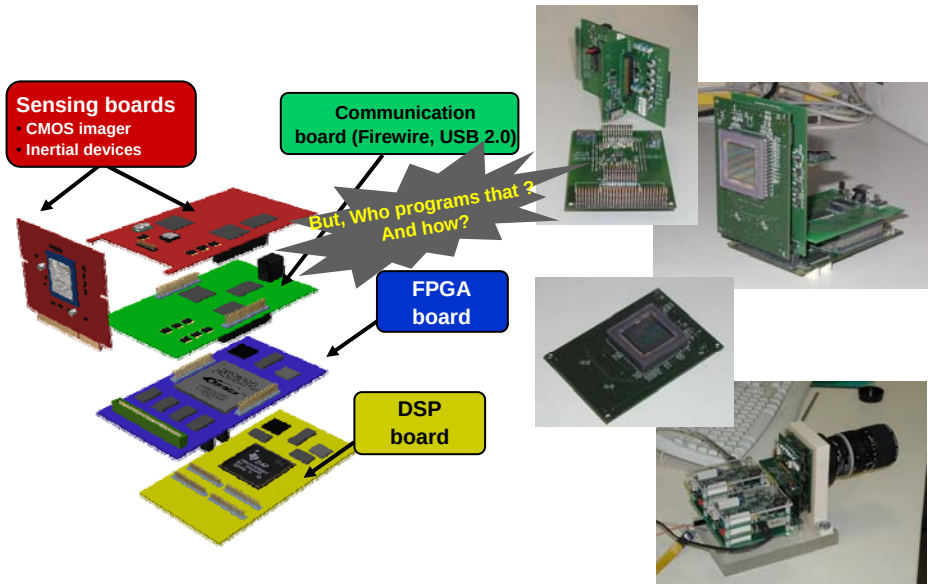
A very efficient smart cam could be based on an efficient mix of FPGA, DSP, GPU !

Architecture of SeeMos Camera



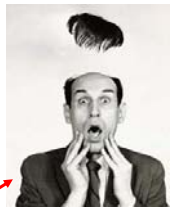
http://wwwlasmea.univ-bpclermont.fr/Personnel/Francois.Berry/seemos.htm

SeeMos Camera



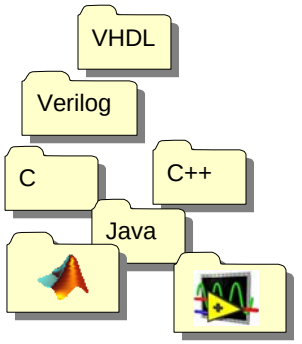
Software Tools

Many devices



Nice Developer

Many tools and ….



… heterogonous languages

Software Tools

Processor (DSP, GPU, Media,…) → **Programming language: C, C++, Java, Matlab, …**

Processor (DSP, GPU, Media,…) → **GUI: Simulink, Labview,…**

Programmable Logic (FPGA,…) → **Description language: VHDL, Verilog,…**

What is a Hardware Description Language (HDL)?

- A textual approach to describing electronic circuits
- Not limited to circuit structure, can describe temporal/operational behavior
- Can be very efficient (RTL level), but not really easy to use!!

- Thinking in hardware terms and not in algorithmic terms
- Need a very good knowledge of the low level hardware

Open Problems

- Efficient HW/SW partitioning (Co-design)
  - Boundary between SW and HW is fixed
  - FPGA performance is dependent on high-level architecture and low-level details
  - Compilation times for FPGA changes can be long
  - Abstractions are not mature

SeeMos Camera Software Development

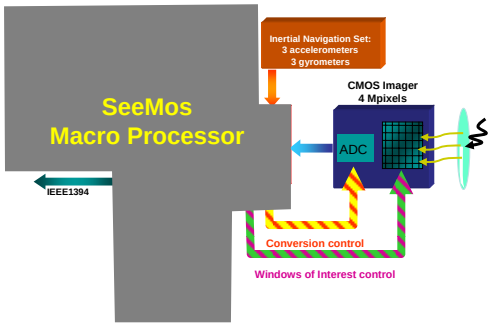
Our hardware is composed by 1 DSP 1 FPGA => heterogonous architecture

Difficulties of programming
(only for specialists ! ;))

Our solution: Describe the whole system processing (DSP+FGPA) like macro processor with a dedicated instructions set based on vision processing

PhD Thesis of
Fabio Dias Real

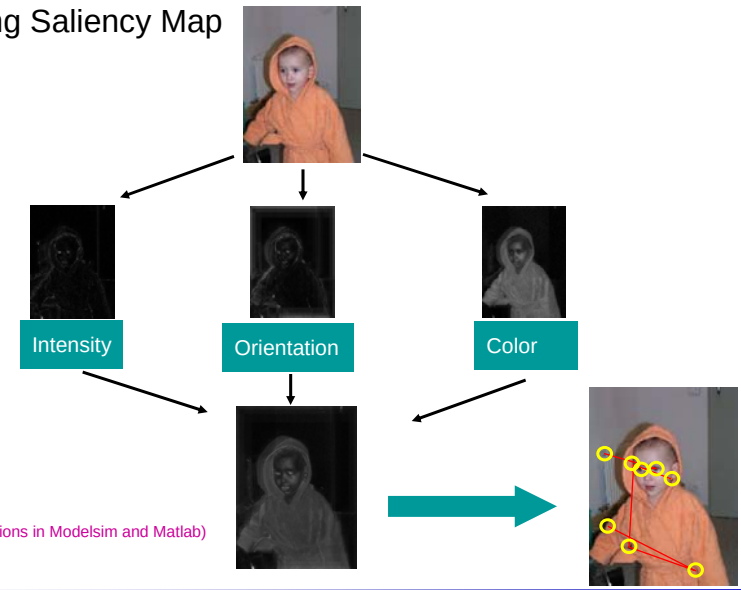
SeeMos Camera Software Development



- SeeMOS Macro Processor is a Functional Processor model
- This functional model is composed of a generic part (control) and a customized part
- The user only needs to program the macro processor in a high level language
- The challenge is to propose an efficient macro processor mapping on the hardware

Example Applications

Computing Saliency Map



(simulations in Modelsim and Matlab)

Example Applications

Template Tracking

Size of template : 32x32 pixels

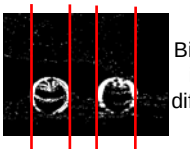
Frame rate : 1000 templ/s

Tracking: SAD on 64x64 pixels

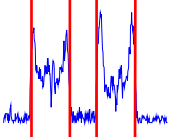
Implemented in VHDL (FPGA)

Example Applications

Motion Detection

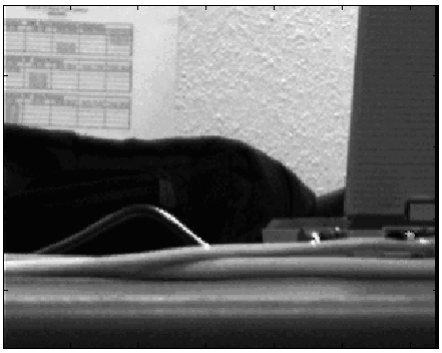


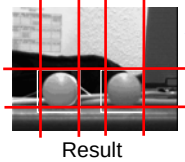
Binarized image difference



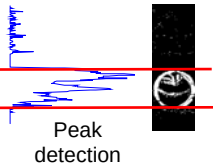
Vertical projection

Peak detection





Result



Peak detection

Horizontal projection (only on detected vertical bands)

Conclusions

- Low-power smart wireless cameras can be designed with SIMD front-ends
- Wireless node opens research challenges for distributed camera networks
- Active vision capable architectures show interesting future capabilities

Outline

I. Introduction
II. Smart Camera Architectures
    1. Wireless Smart Camera
    2. Smart Camera for Active Vision
III. Distributed Vision Algorithms
    1. Fusion Mechanisms
    2. Vision Network Algorithms
IV. Requirements and Case Studies
V. Outlook