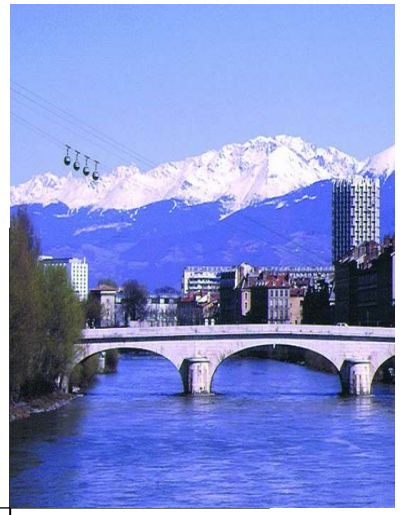
Smart Cameras and Visual Sensor Networks



Smart Camera and Smart imager

François BERRY - LASMEA CNRS
Dominique GINHAC – LE2I

EMBEDDED SYSTEMS WEEK

ALPEN-ADRIA UNIVERSITÄT KLAGENFURT

LASMEA

LABORATOIRE DE RECHERCHE EN INFORMATIQUE

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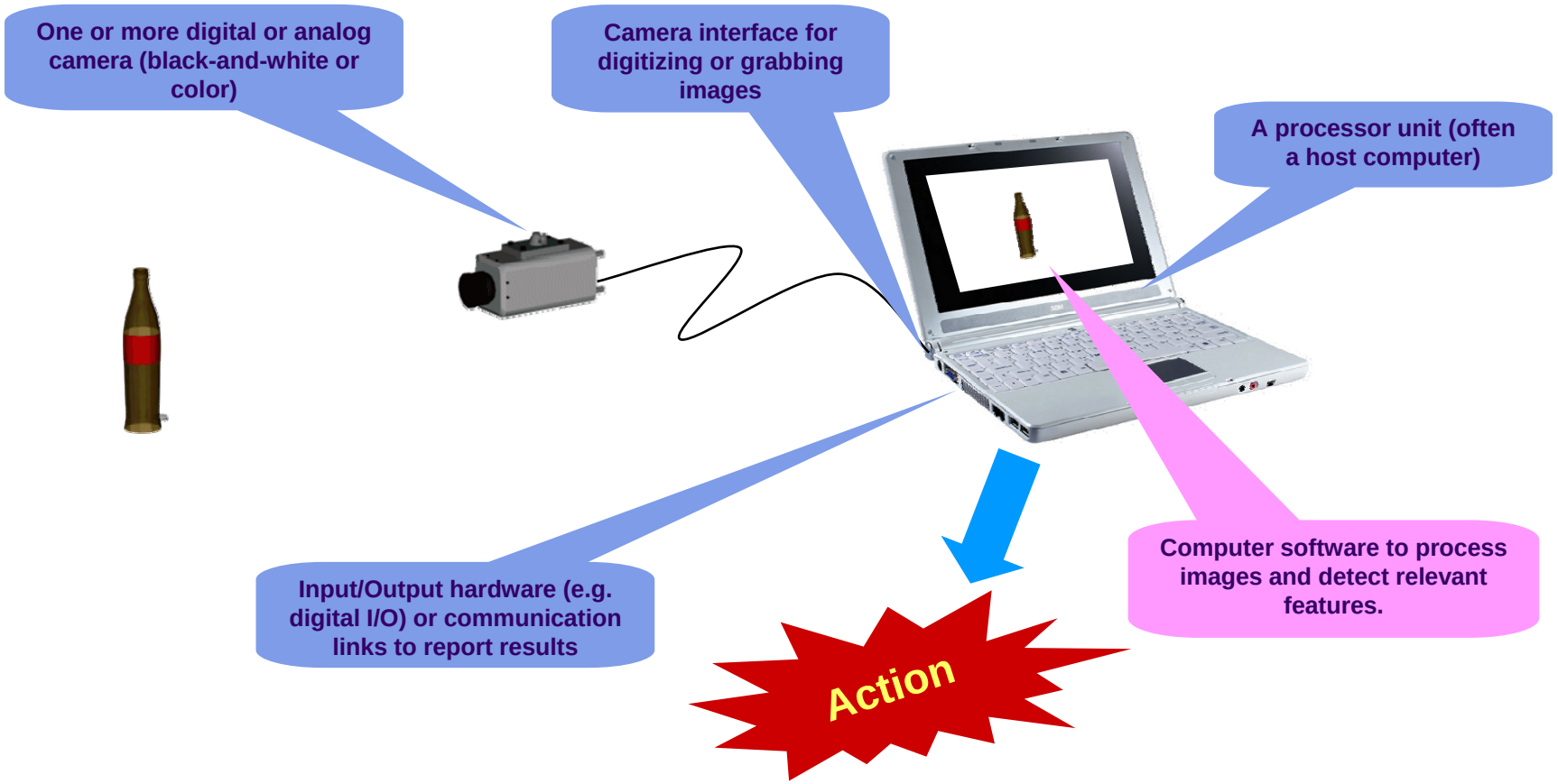
Machine vision system

A traditional machine vision system consists of :



Introduction

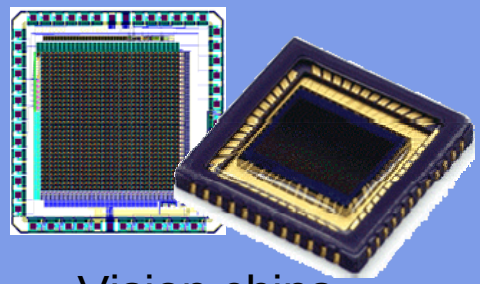
But a machine vision can also be integrated in an embedded system under 2 levels:

System-level

Smart Camera

Example: surveillance,…

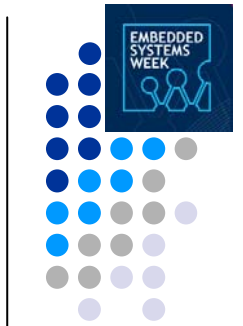
Chip-level



Vision chips
or
Smart Imager

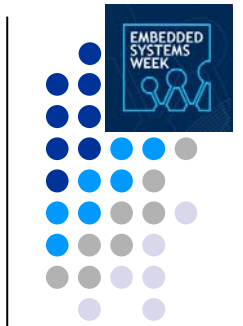
Example: optical mouse,…

Smart Imagers & Smart Camera



- Smart cameras
- Smart imagers and Vision chips

Smart Imagers & Smart Camera



- **Smart cameras**
  - Definition
  - Imaging devices
  - Communication
  - Processing
- **Smart imagers and Vision chips**

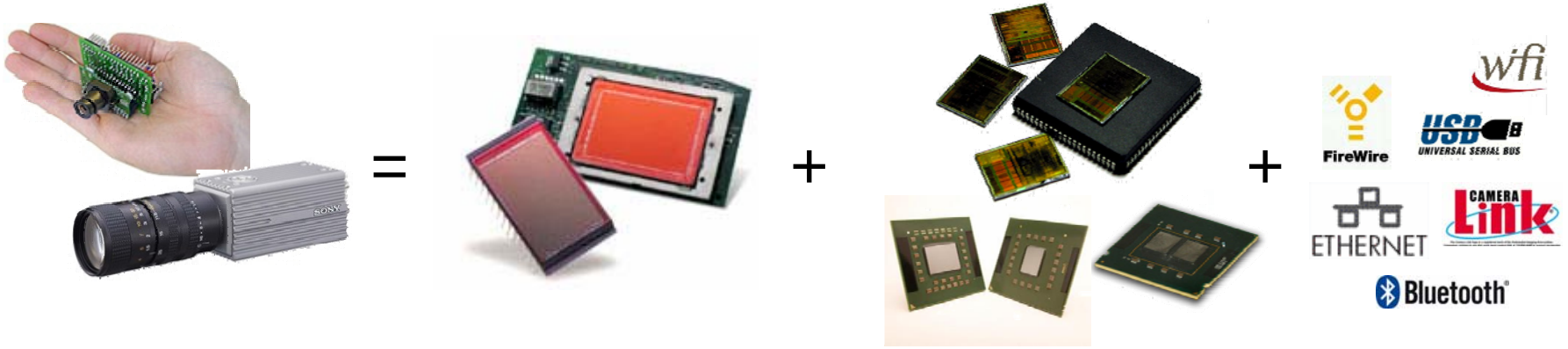
Smart camera

A definition

Source: Wikipédia

A **smart camera** is an embedded machine vision,

- in addition to image capturing circuitry,
- includes a processor, which can extract information from images without need for an external processing unit,
- interfacing devices used to make results available to other devices.



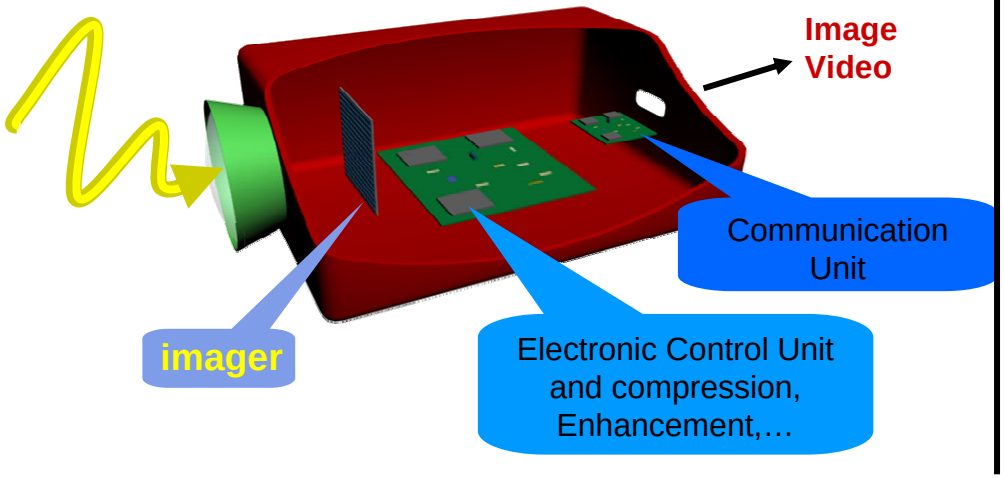
Smart Camera = Σ Capture + Processing + Communication

Smart camera vs traditional camera

Traditional camera

- Imager
- Electronics
- Interfaces

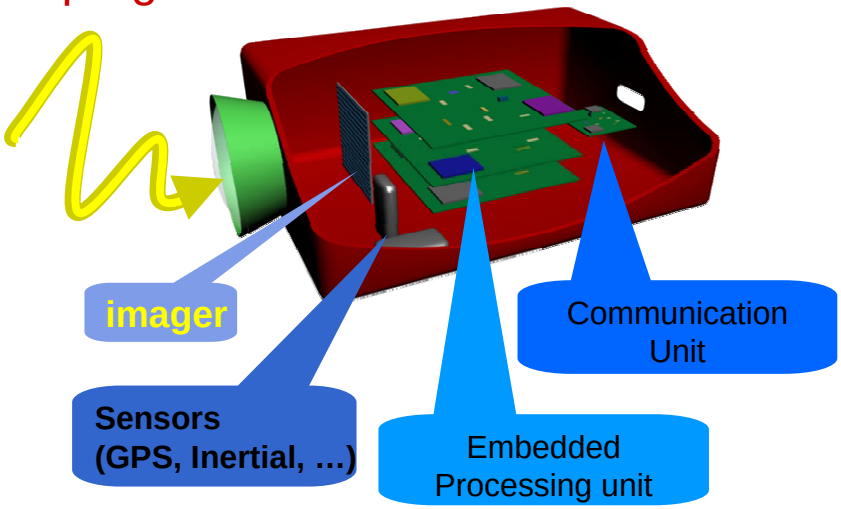
Traditional camera provides images and videos.



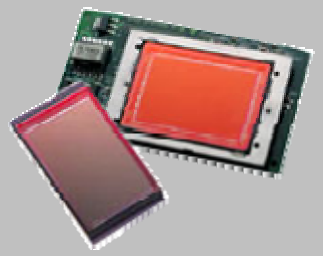
Smart camera

- Imager (and sensors)
- Onboard computer
- Interfaces

Smart camera delivers abstracted image data and is also configurable and programmable



Anatomy of a smart cam



Sensing devices:

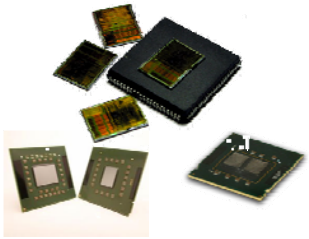
Imager: CMOS, CCD,…

Proprioceptive devices: Inertial set,…

Communication unit:

Wireless: Wifi, Bluetooth, ZigBee…

Wired: USB, FireWire, Ethernet Gigabit, Camlink,…



Processing Unit:

Micropocessor

DSP

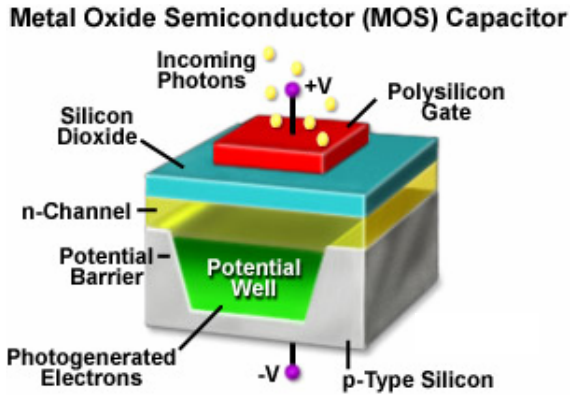
FPGA

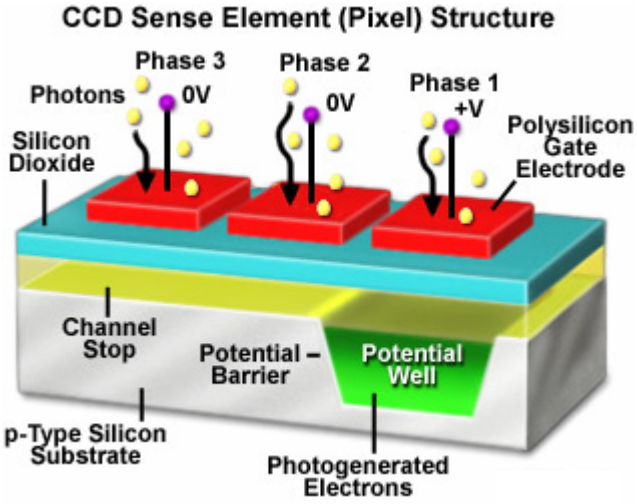
ASIC, GPU,…

Imaging devices: CCD vs CMOS

CCD imager consists of a large number of light-sensing elements arranged in one or two-dimensional array on a thin silicon substrate.

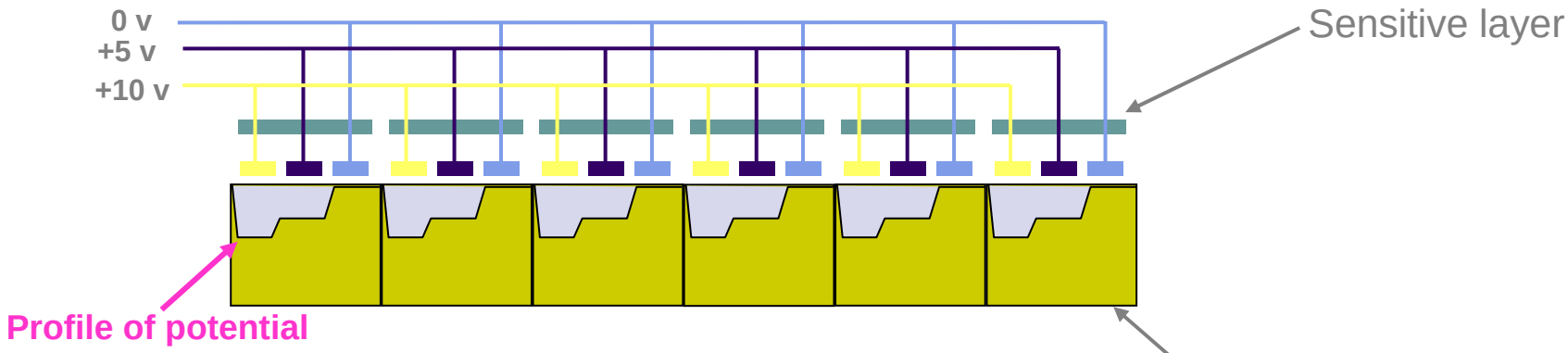
The fundamental light-sensing unit of the CCD is a metal oxide semiconductor (**MOS**) capacitor operated as a photodiode and storage device





CCD imager (Charge Coupled Device)

- **Photons release electrons (photoelectric effect)**
- **Electrons emitted by photosensor during capture are stored in a potential well**
- **At the end of the field, potential of the read-out gate is lowered and electrons pass into the shift register.**



Principle of the CCD imager

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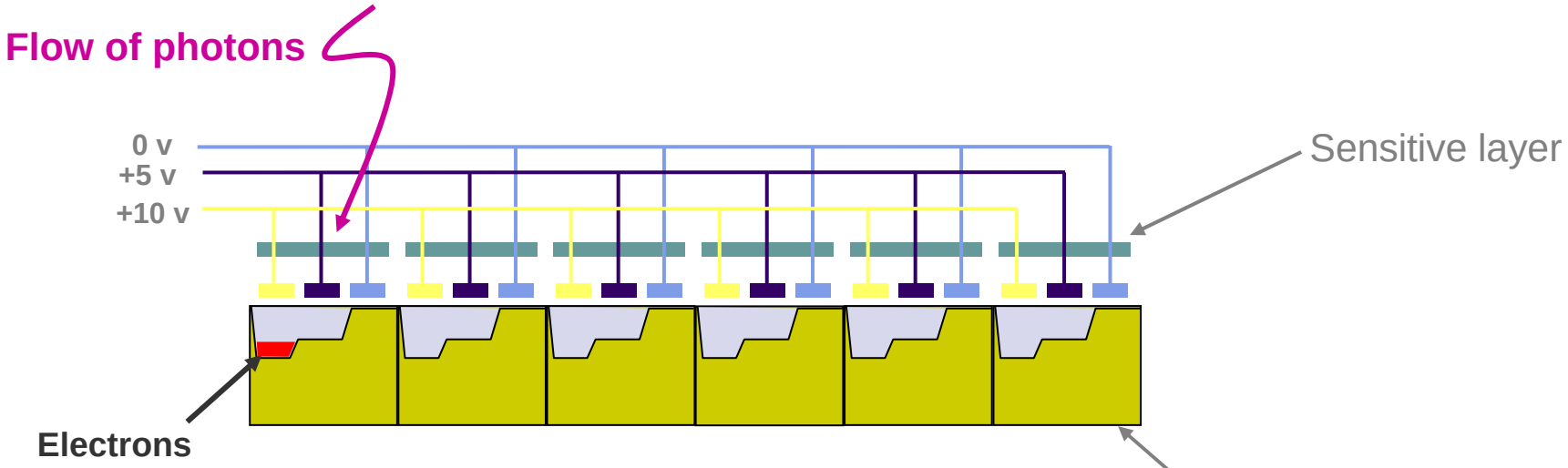

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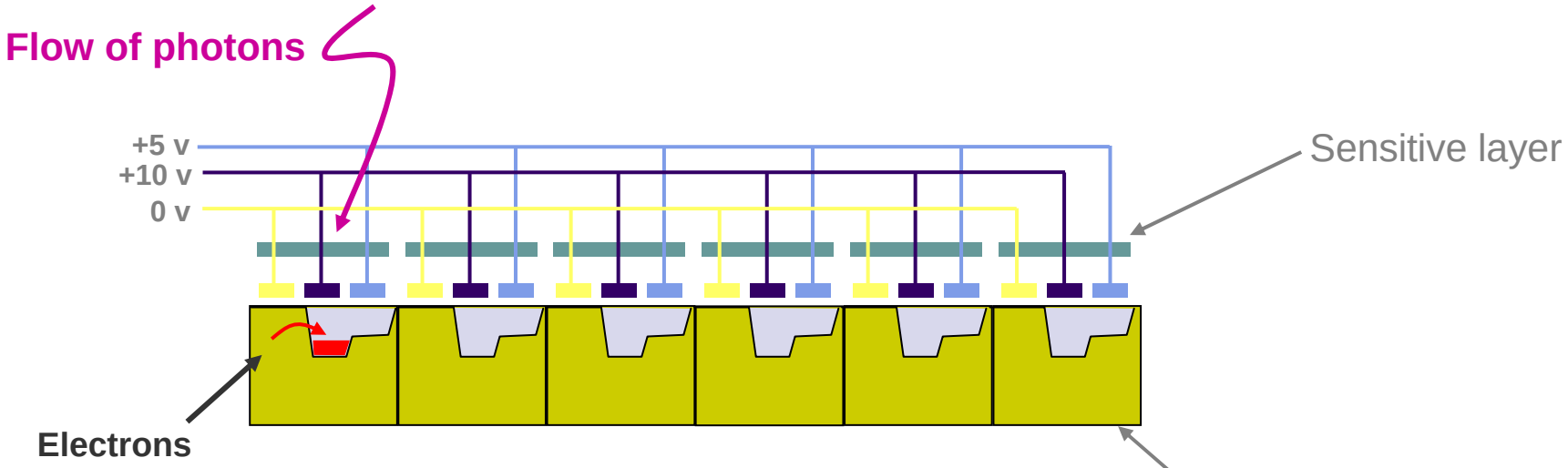

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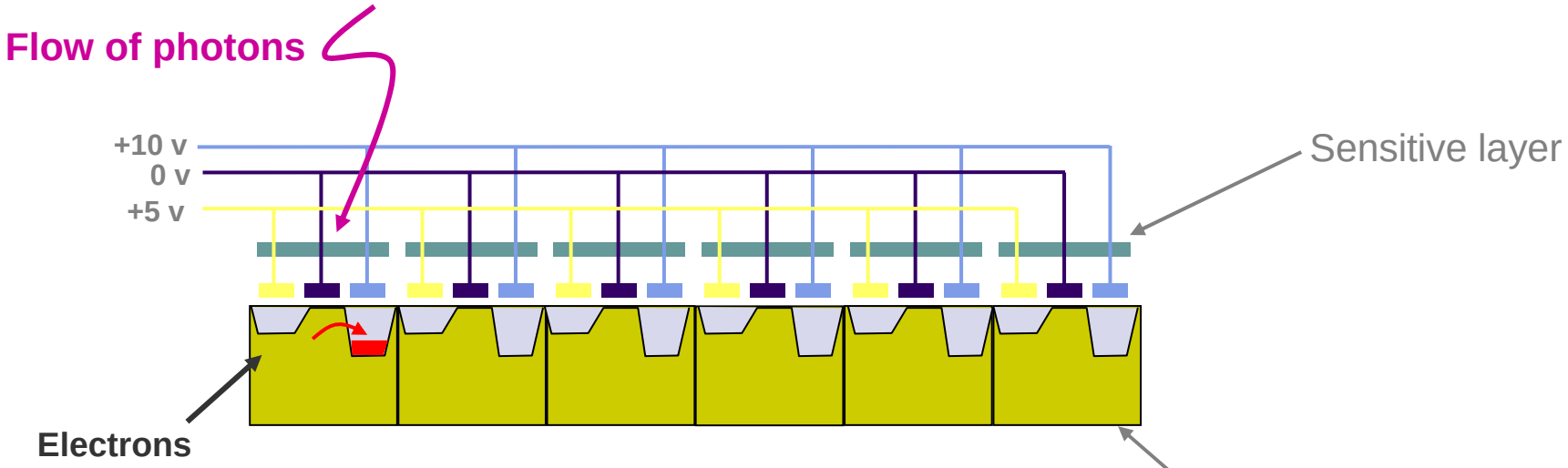

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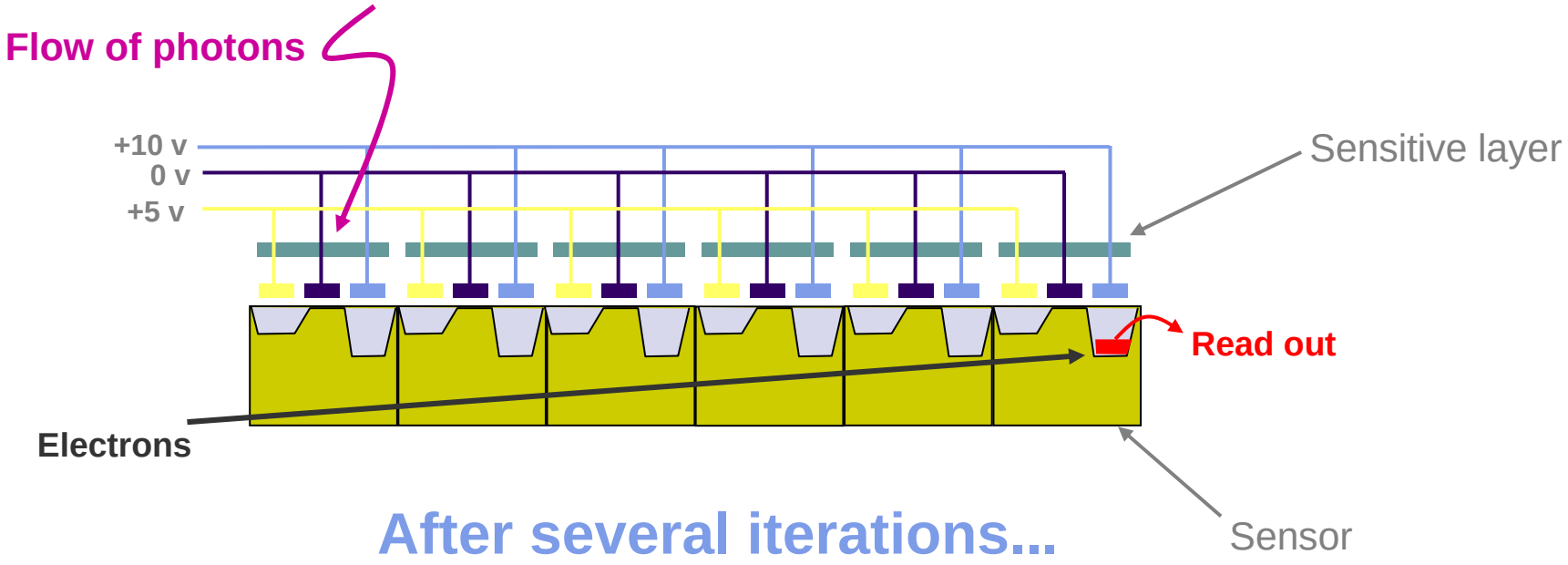

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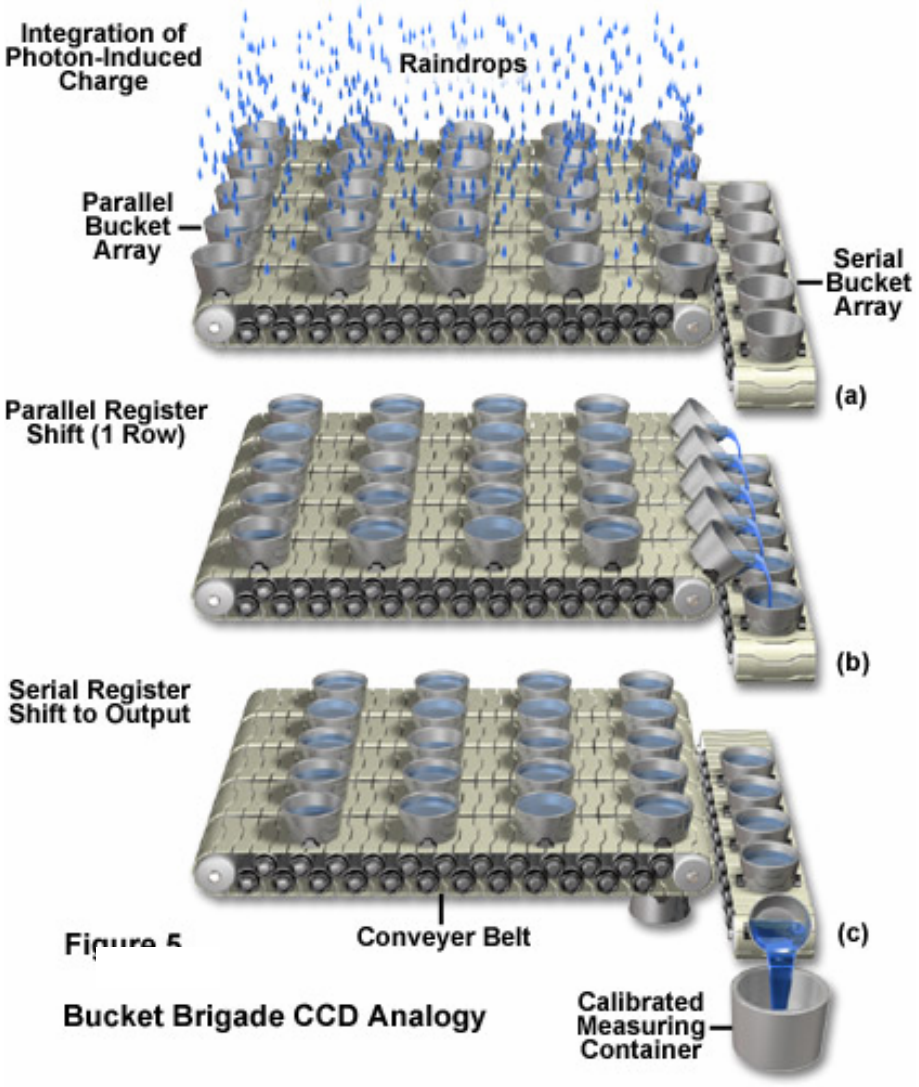


Figure 5

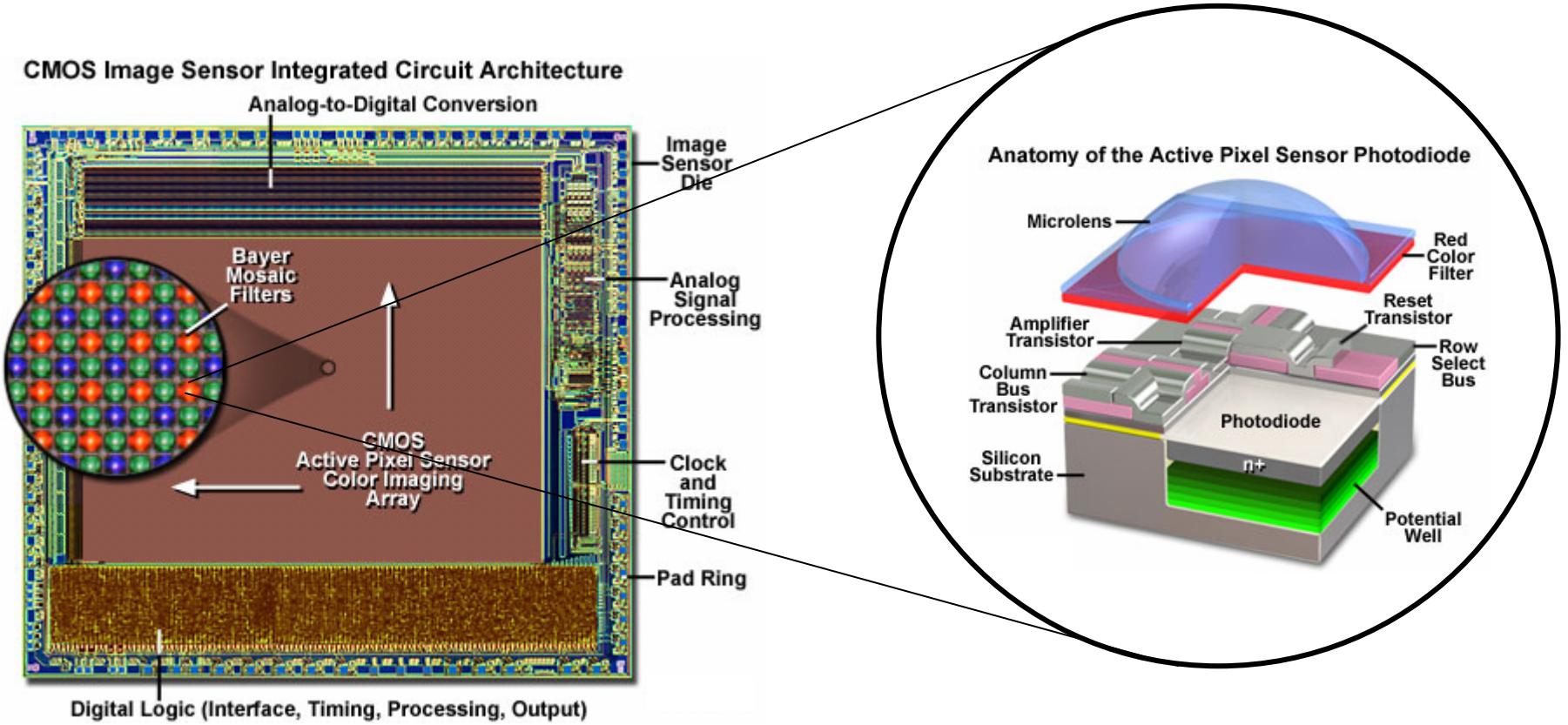
Bucket Brigade CCD Analogy

Water Analogy

With each complete parallel transfer, charge packets from an entire pixel row are moved into the serial register where they can be sequentially shifted toward the output amplifier, as illustrated in the bucket brigade analogy

CMOS Imager

The major advantage that **CMOS imagers** enjoy over their CCD counterparts is the ability to **integrate a number of processing and control functions** directly onto the sensor integrated circuit, which lie beyond the primary task of photon collection.



Imaging devices: CCD vs CMOS

	CCD	CMOS standard
Noise	Low	Moderate
Cost	High (dedicated process)	Low (volume)
Output	Serial	Random access
*Power needed**	High	Low (CMOS)
Speed	Moderate to high	Higher
Photo detection	MOS Capacity	Transistors
Clocks	Multiple	Single
Integration	Hard	Easy

***A typical CCDs consumes 2 to 5W of power, a CMOS chip typically 20mW to 50mW**

Source : http://www.dalsa.com/shared/content/Photonics_Spectra_CCDvsCMOS_Litwiller.pdf

Others sensing devices

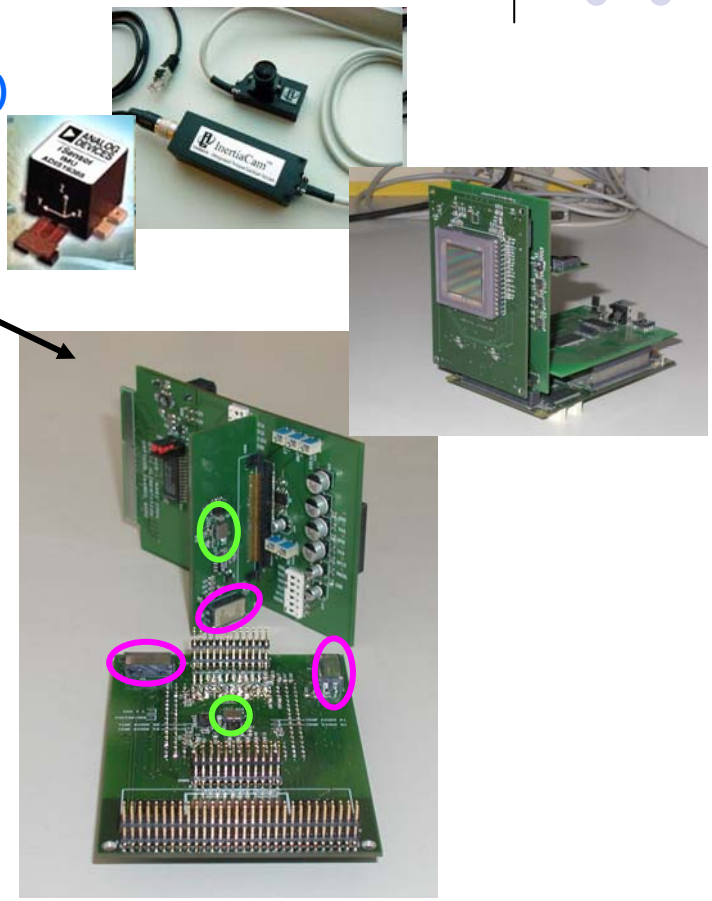
Imaging unit can be improved by others sensors such as:

- Inertial measurement unit:

(3 linear accelerations and 3 rotational velocities)

Used for:

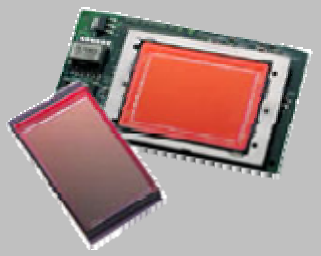
- **Image stabilization**
- **Inertial and Image fusion**
- **Inclinometer (with gravity)**
- **….**



- GPS module

provides reliable positioning, navigation, and timing services

Anatomy of a smart cam



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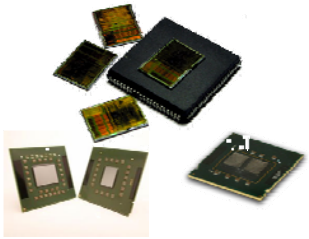


Processing Unit:

Micropocessor

DSP

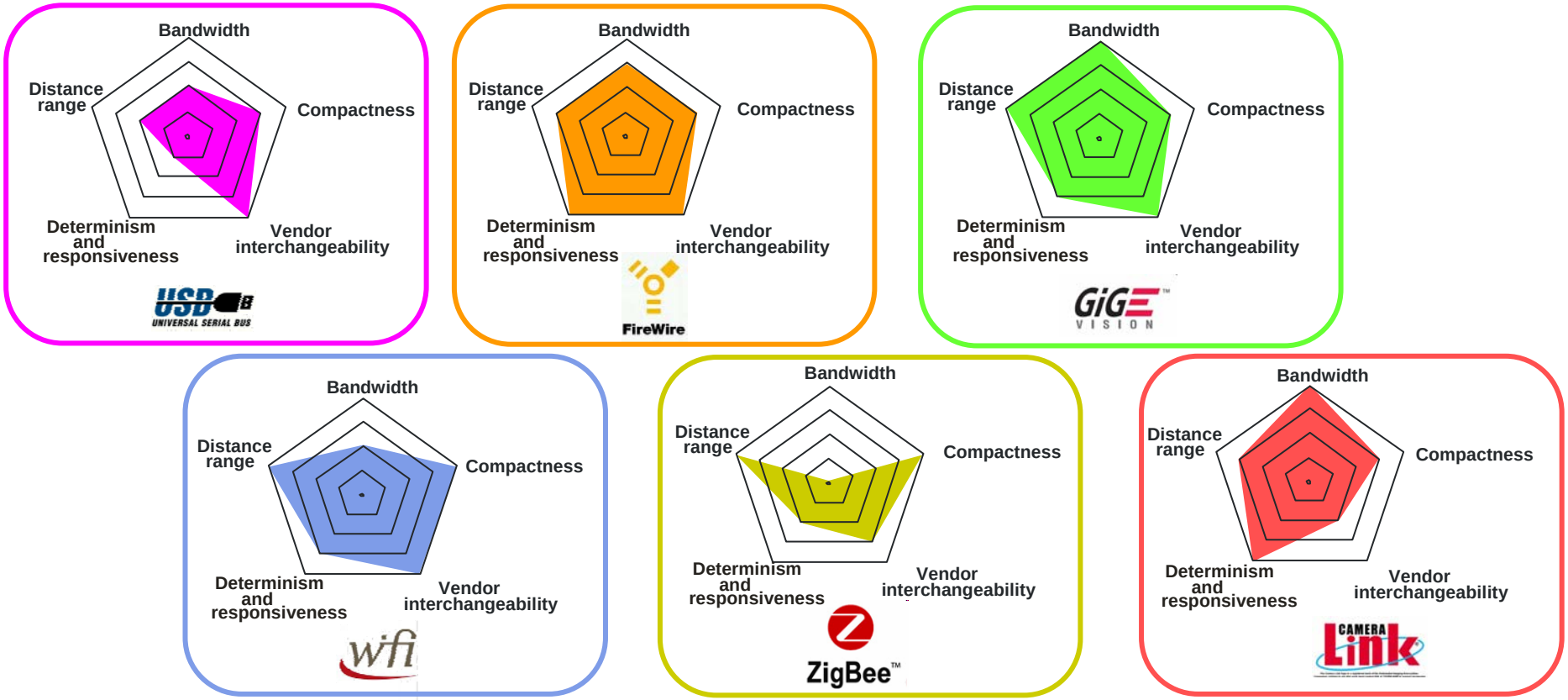
FPGA

ASIC, GPU,…

Taxonomy of Communication units

Communication channel can be classified according to 5 factors (not exhaustive!):

- ***Bandwidth***
- ***Distance range***
- ***Compactness***
- ***Determinism and Responsiveness***
- ***Vendor interchangeability***



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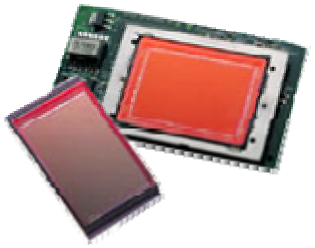

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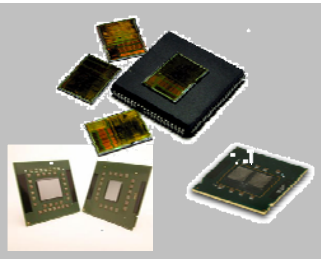


Processing Unit:

Micropocessor

DSP

FPGA

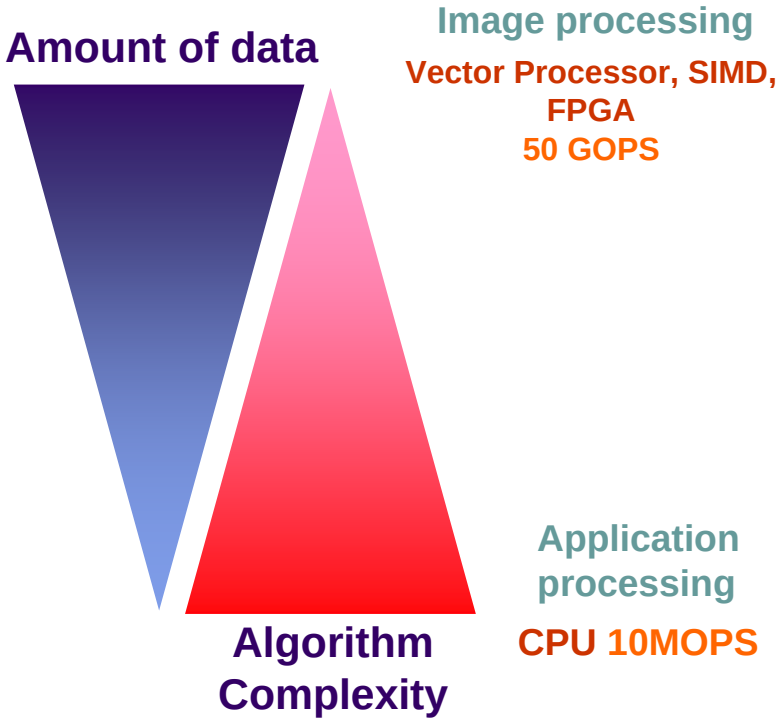
ASIC, GPU,…

Processing Unit

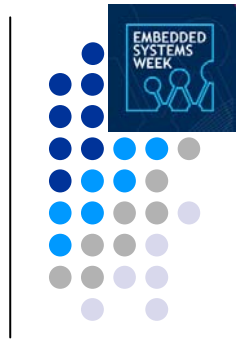
The objective of Vision system is to measure different features of a specific object.
As every image contains a lot of unnecessary information,
so the ____ key is data reduction.

Mostly image processing tasks can be divided into 3 levels:

- **Parallel data reduction, where the operations depends on the closest surroundings (e. g. noise reduction, edge detection).**
- **Serial data reduction, where data from the entire image is needed for the processing task (e. g. count the number of elements).**
- **Classification, that try to inform what we see.**



Processing Unit: What do we need?



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(noise reduction, edge detection).

- Serial data reduction, where data from the entire image is needed for the processing task (e. g. count the number of elements).

- Classification, that try to inform what we see.

Image processing
Vector Processor, SIMD, FPGA
50 GOPS

Application processing
CPU 10MOPS

Processing Unit: What are the constraints?

Smart Camera

Embedded system

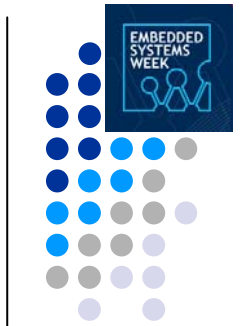
Differentiating features:
- **power**
- **cost**
- **speed (must be predictable)**

Runs a few applications often known at design time

Not end-user programmable

Operates in fixed run-time constraints (Real time)

Processing Unit: Which kinds of technology?



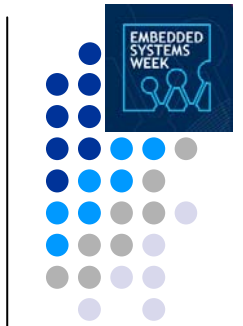
Technology

Processor approach:
DSP,
Media Processor,
GPU,
General Purpose Proc,…

Programmable Logic approach:
CPLD, FPGA

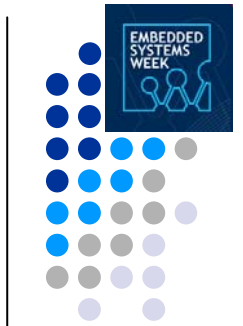
More details in next part of tutorial

Smart Imagers & Smart Camera



- **Smart cameras**
  - Definition
  - Imaging devices
  - Communication
  - Processing
- **Smart imagers and Vision chips**

Smart Imagers & Smart Camera

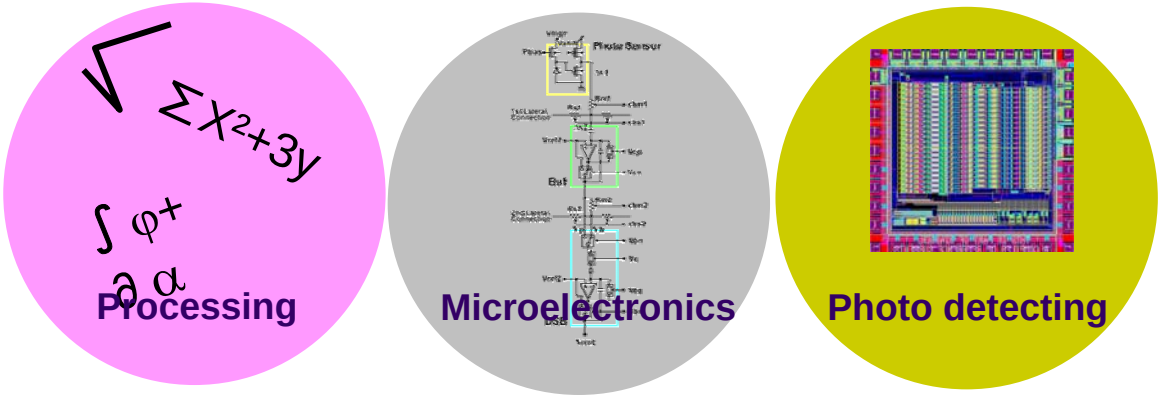


- **Smart cameras**

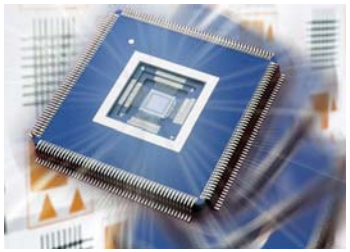
- **Smart imagers and Vision chips**
  - Definition
  - Various pixels
  - Famous imagers

Vision Chips (Seeing silicon)

Integration of photo detecting elements and processing circuits on the same chip, to obtain better performance from sensors



A good bib. reference:
Vision chip by A. Moini - Kluwer

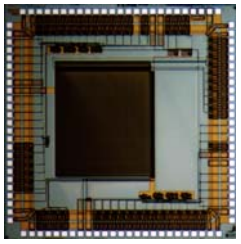


Vision chip

Vision Chips (Seeing silicon)

Two main approaches:

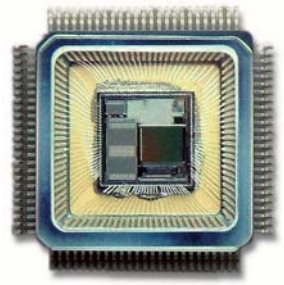
Smart sensor: It is a “photo detector-level processor”.
Smart-sensors are information sensors, not only transducers and signal processing elements.



- Mostly analog processing
- Pixel size (fill factor) implies simple process
- Everything in a smart sensor is specifically designed for the targeted application.

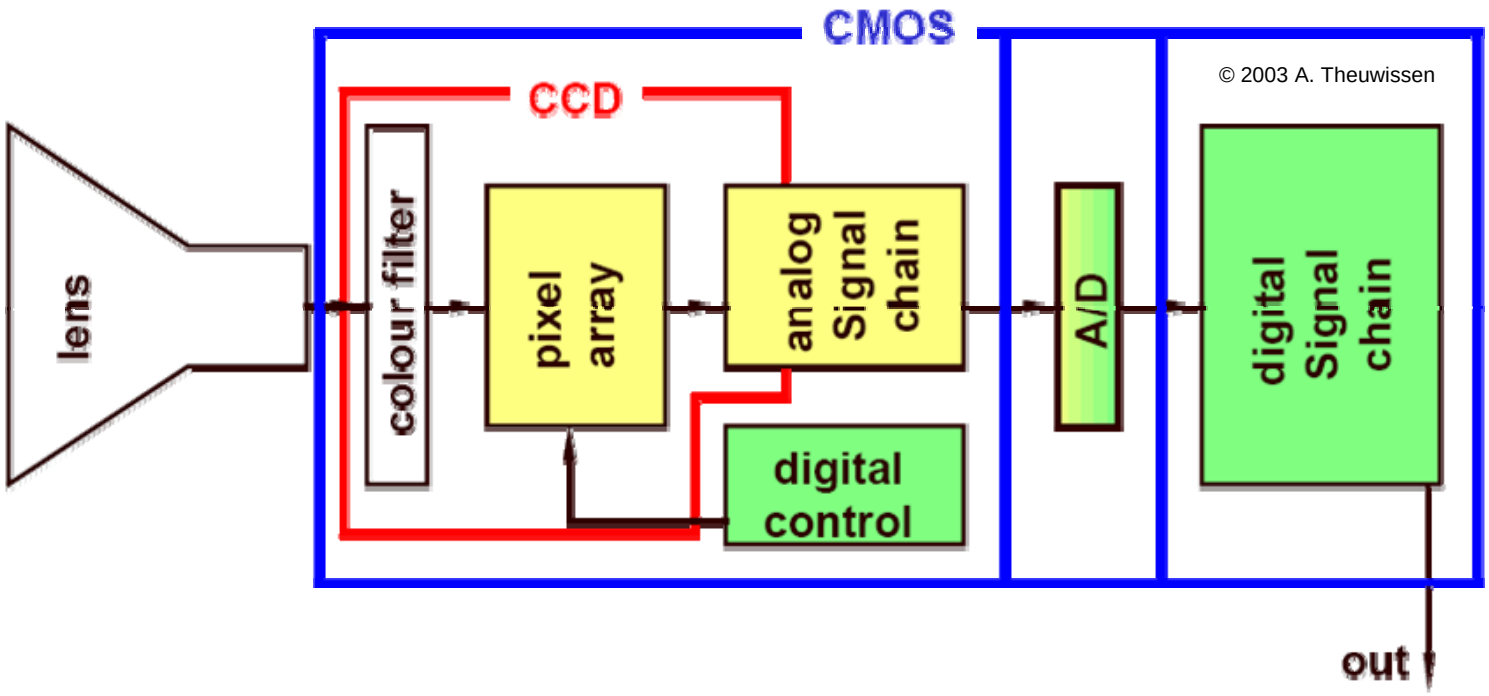
- **Vision System On Chip:**

The integration of an imager (CMOS) and processing circuits on the same chip, to make sensing and processing system more compact



- Analog and digital processing
- Chip size is a limitation for the processing
- First step towards smart cam

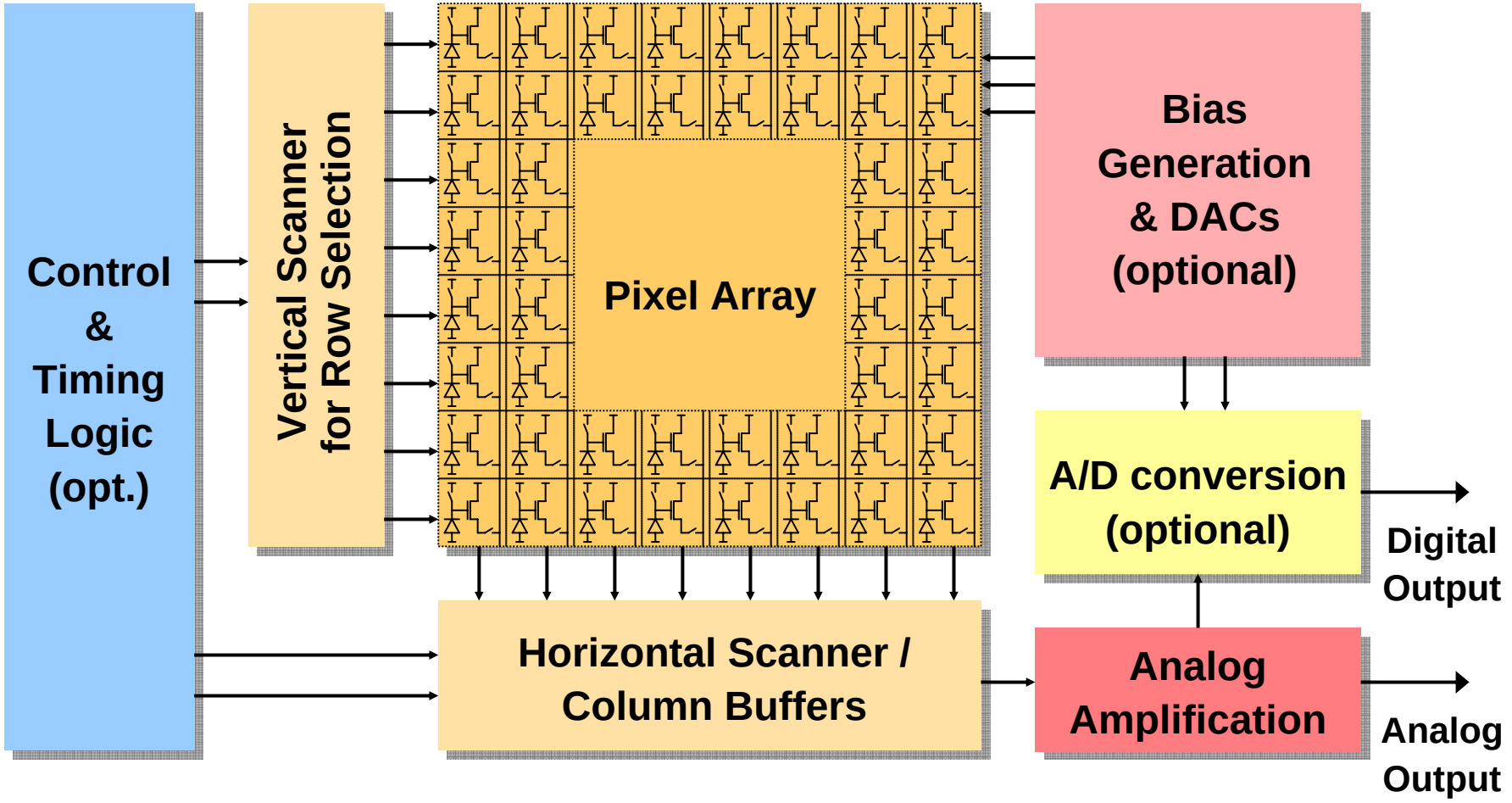
CMOS vs CCD : from sensor to VSOC



The main difference between CMOS and CCD imagers is the degree of integration available to the designer

- **A CCD is only comprised of the pixel array and an analog output stage**
- **A CMOS imager may consist of not only the pixel array and the analog stage, but also complete analog signal chain as well as complete digital processing stage**

General Architecture of CMOS-Based Image Sensors



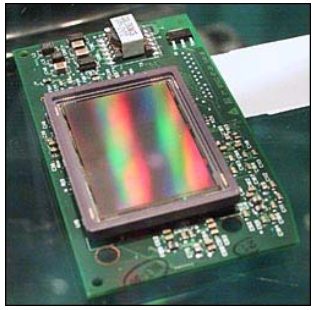
Common CMOS features

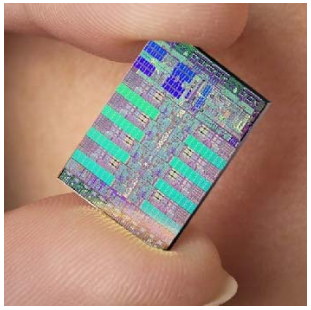
CMOS sensors use the same technological process as modern microchips:

- Many foundries available worldwide
- Cost efficient
- Latest processes available down to 90 nm

CMOS process enables integration of many additional features:

- Random pixel access, windowing, subsampling and binning
- Various pixel circuits from 3 transistors up to many 100 transistors per pixel
- Analog signal processing (e.g. CDS, programmable gain, noise filter)
- A/D conversion
- Logic (timing control, digital signal processing, etc.)



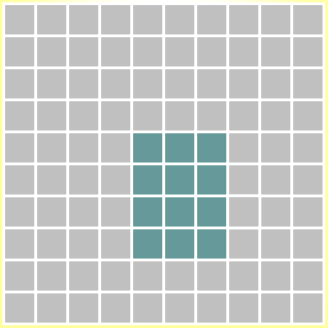


Random pixel access

- **Different scanning methods are available to reduce the number of pixels being read:**
  - **Allows for higher frame rate or lower pixel rate (reduction in noise)**
  - **Can reduce power consumption due to reduced data**

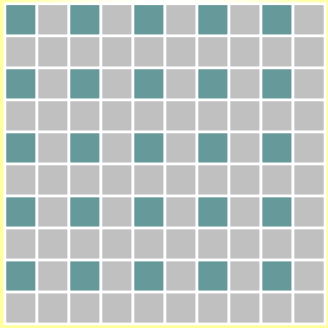
Windowing

- Reading of one or multiple rectangular subwindows
- Used to achieve higher frame rates (e.g. AO, guiding)



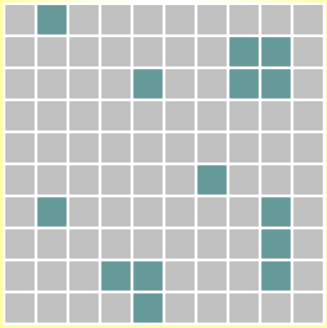
Subsampling

- Skipping of certain pixels/rows when reading the array
- Used to obtain higher frame rates on full-field images



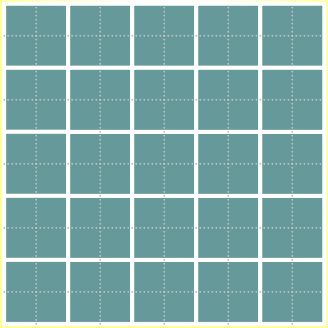
Random Read

- Random access (read or reset) of certain pixels
- Selective reset of saturated pixels
- Fast reads of selected pixels



Binning

- Combining several pixels into larger super pixels
- Used to achieve lower noise and higher frame rates



Various pixels

Passive Pixel Sensor (PPS)

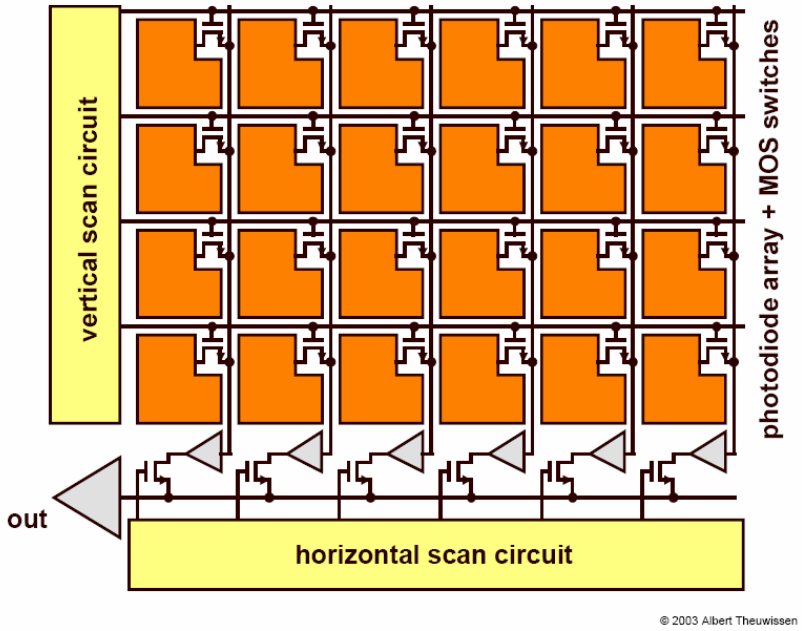
- Architecture very similar to a SRAM or DRAM chip
- Row of pixels can be addressed through the vertical scan circuit and then a single pixel of the selected row can be addressed with the horizontal scan circuit

Each CMOS pixel based on:

- A photodiode and an addressing transistor that acts as a switch
- Very simple and compact construction

Pros and cons :

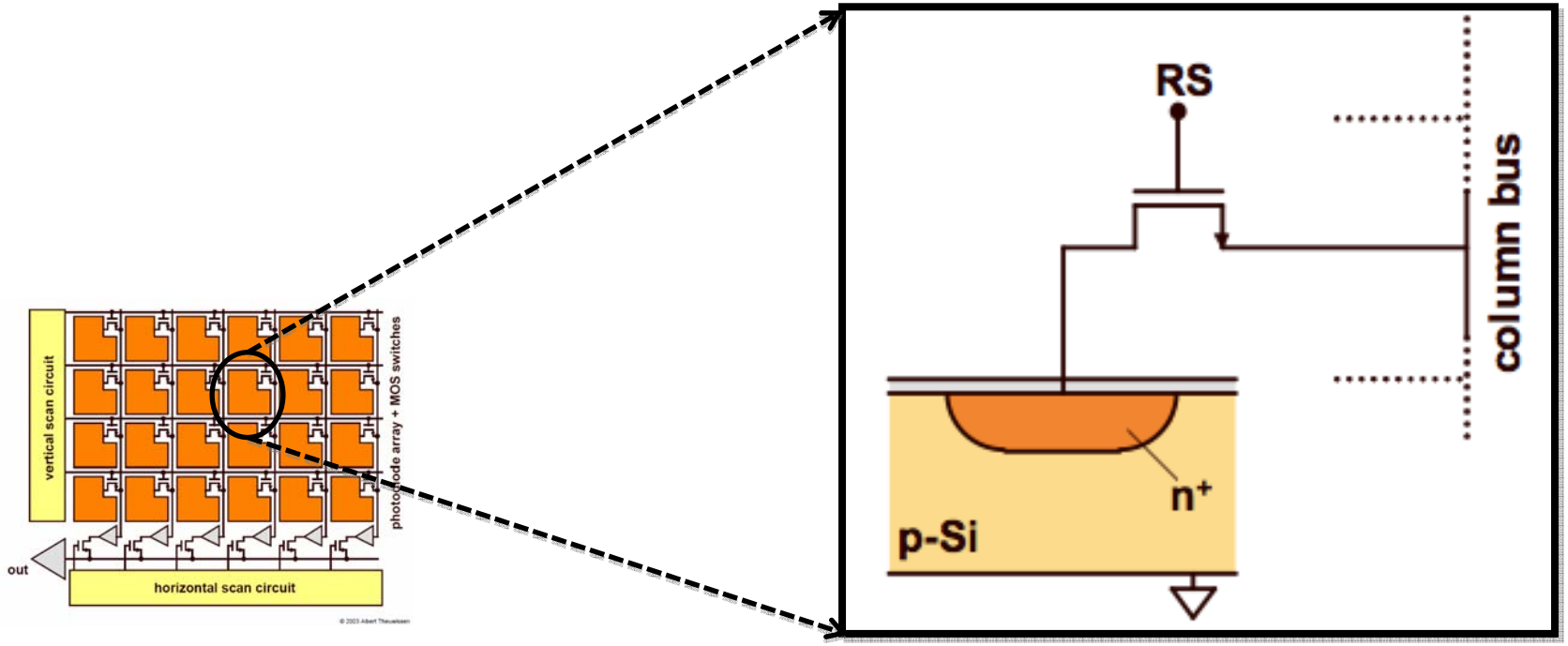
- Fill factor (ratio of diode area to total pixel area) near 100 %
- Each pixel is suffering from a large noise level



Various pixels

Working principle of the Passive Pixel Sensor (PPS)

- First, the photodiode is reverse biased to a high voltage
- During the exposure time, photons decrease the reverse voltage across the photodiode
- At the end of the exposure time the remaining voltage is measured, and its drop from the original value is a measure for the amount of photons falling on the photodiode during the exposure time



Various pixels

Active Pixel Sensor (APS)

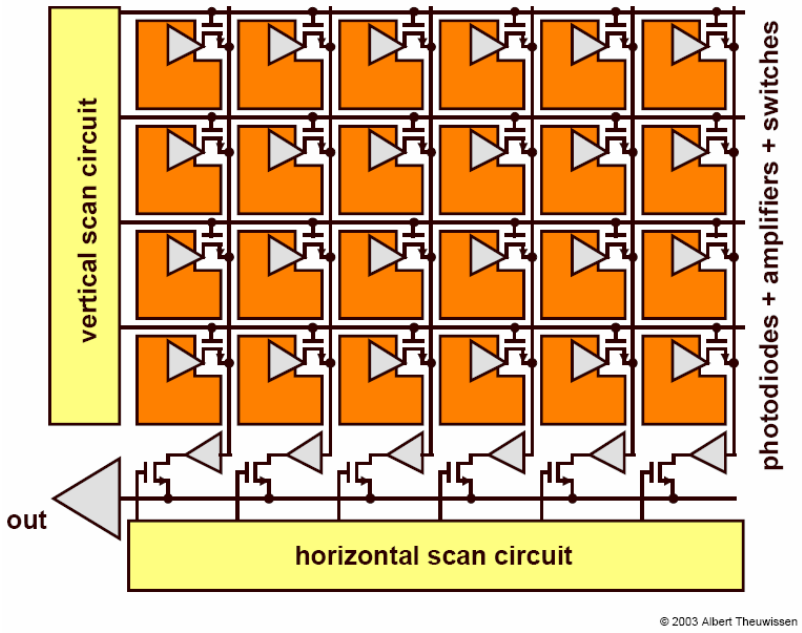
- Major improvement in the noise performance of the pixels
- Every pixel gets its own individual amplifier
- APS architecture is the preferred choice for 2D CMOS image sensors

Each CMOS pixel based on:

- A photodiode, a reset transistor, an amplifier and the addressing transistor

Pros and cons :

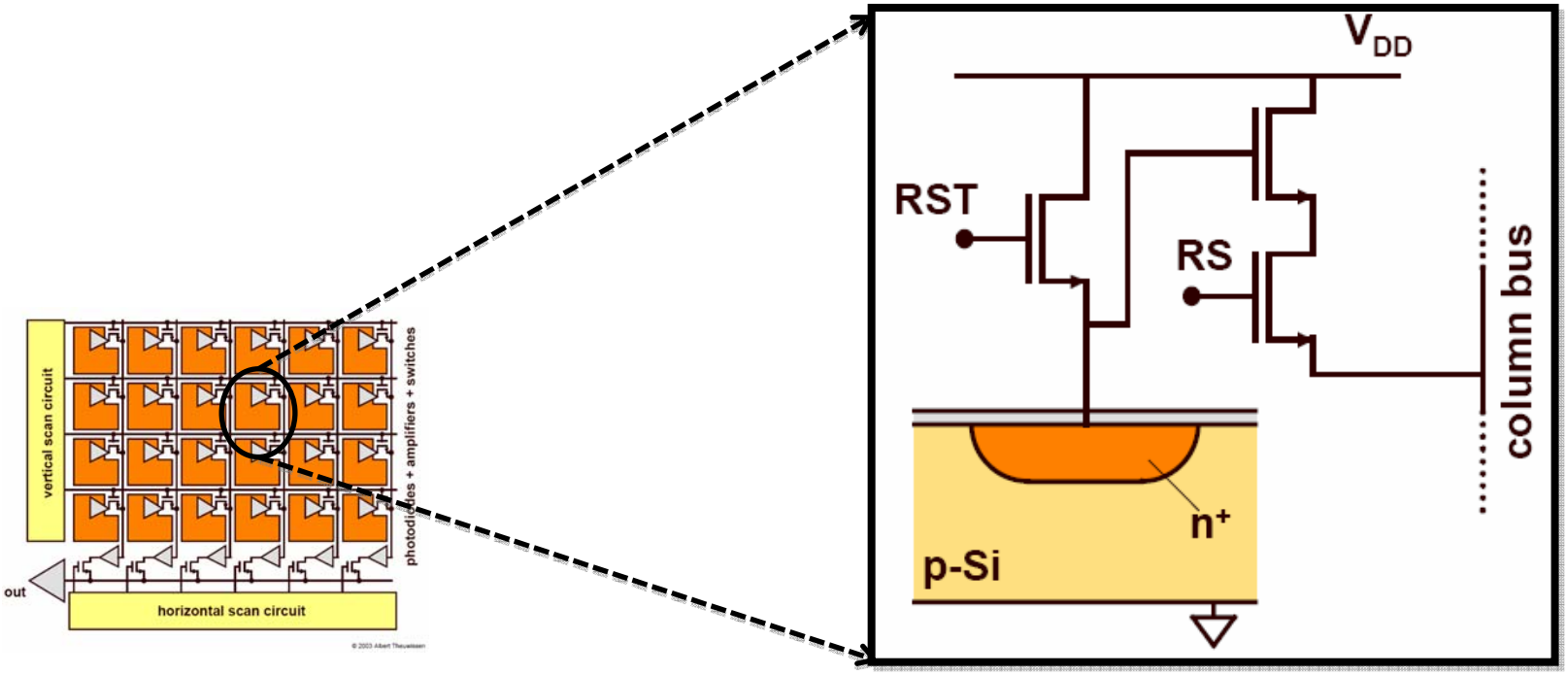
- High value of Fill factor (ratio of diode area to total pixel area)
- Solves a lot of noise problems associated with the PPS approach
- Still suffers from a large reset noise componet that is difficult to be removed from the video signal



Various pixels

Working principle of the Active Pixel Sensor (APS)

- Basically the same working principle as of PPS
- The photodiode is reverse biased or reset (RST transistor),
- Photons decrease the reverse voltage across the photodiode,
- At the end of the exposure time, the pixel is addressed (RS transistor) and the voltage across the diode is brought outside the pixel by means of source follower



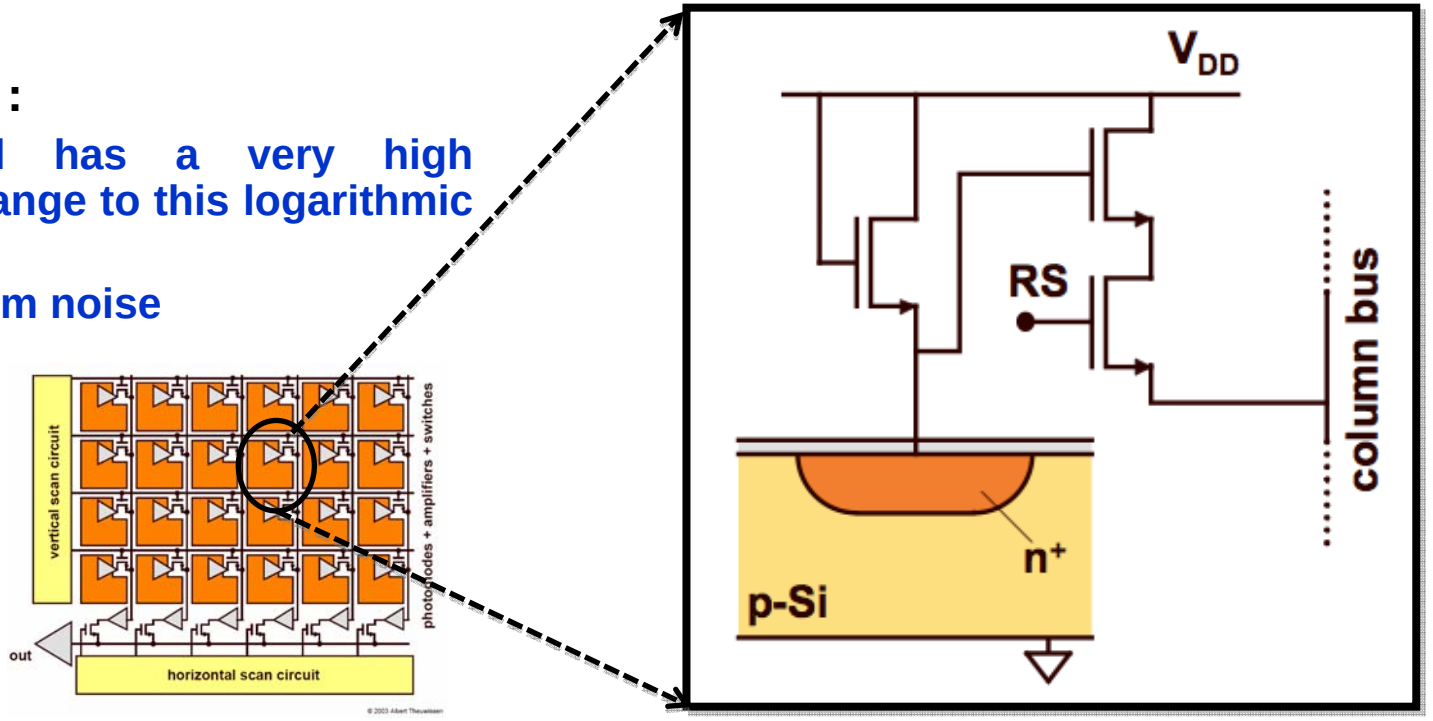
Various pixels

Logarithmic pixel

- Very similar to the basic photodiode 3T APS
- The only difference is the fact that the reset transistor is no longer used in a reset mode, but rather its gate is connected to the drain voltage VDD
- The voltage on the photodiode decreases logarithmically with linear increases in illumination

Pros and cons :

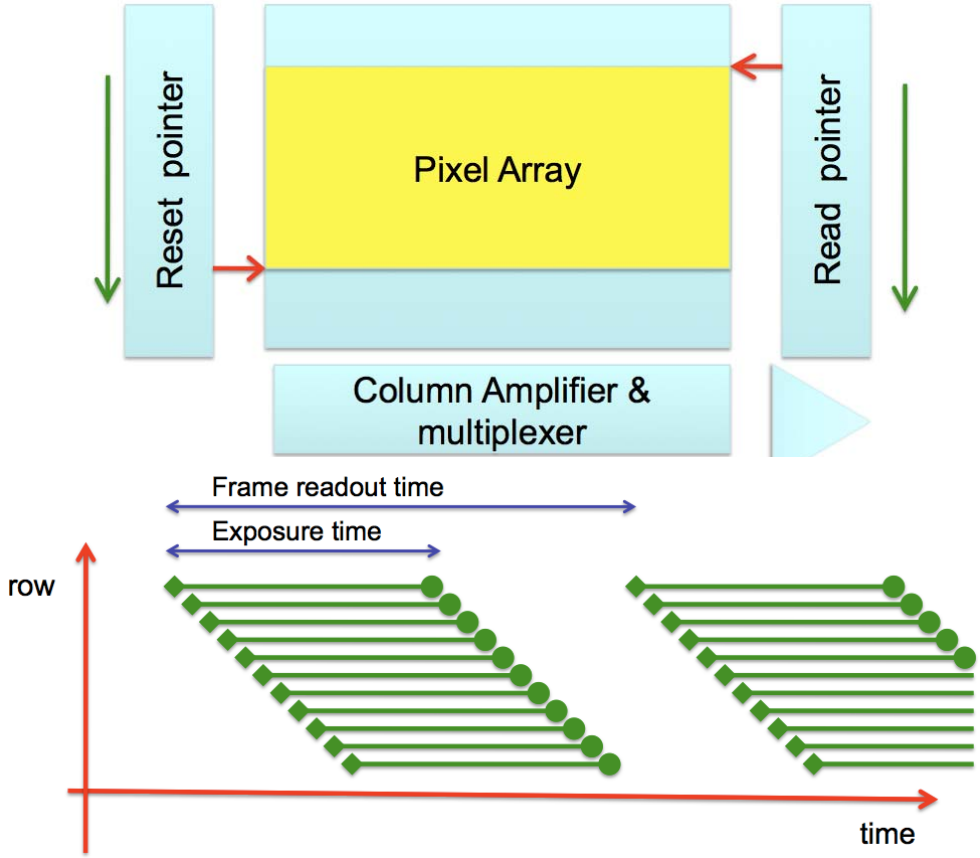
- The pixel has a very high dynamic range to this logarithmic response
- Suffers from noise



Various pixels

Snapshot Active Pixel Sensor (APS)

- Standard APS is based on rolling shutter approach. Where start and end of light collection for each row is delayed by the previous rows.
- Leads to image artefact when motion is present in the image

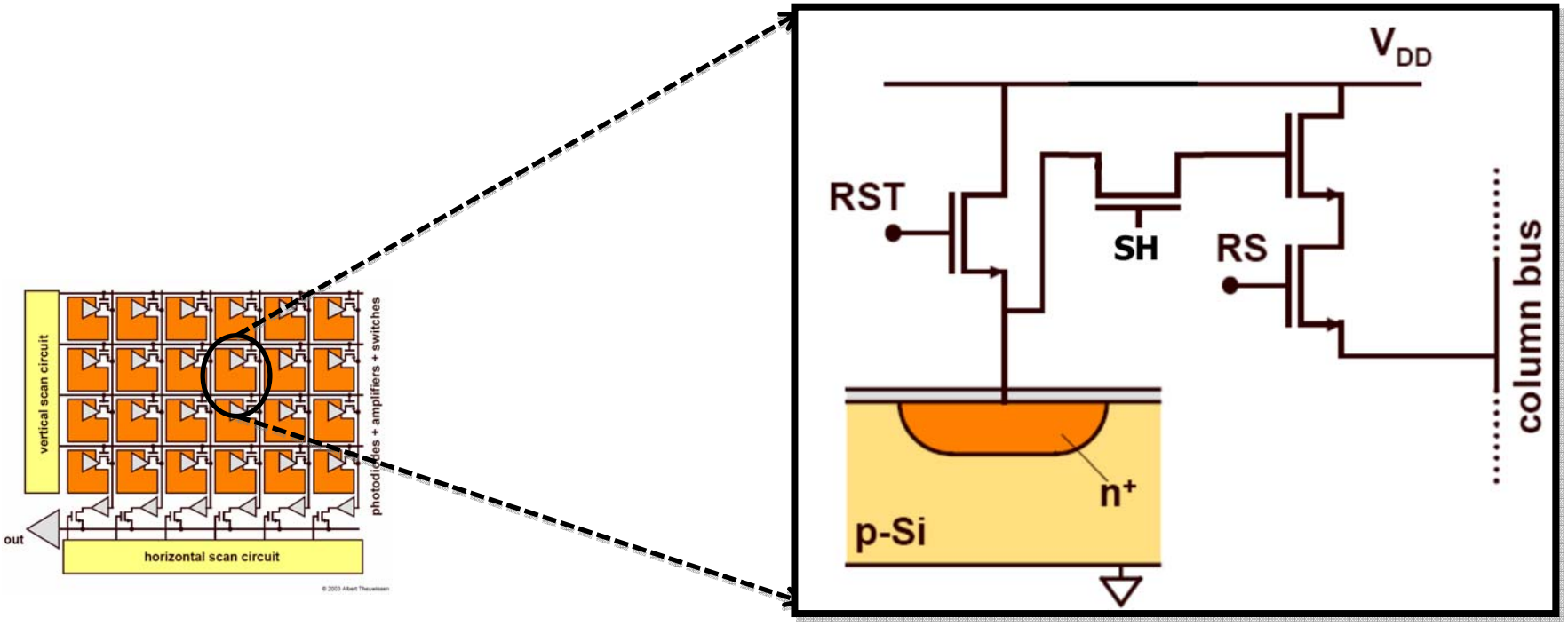


Henry Lartigue, “Race Car »

Various pixels

Snapshot Active Pixel Sensor (APS)

- An electronic global shutter method is required
- Uses an additional transistor (SH)
- After integration, the shutter is opened and the signal charge is stored in the in-pixel sample-and-hold capacitance until readout



Various pixels

Advanced structure of APS: Pinned photodiode pixel

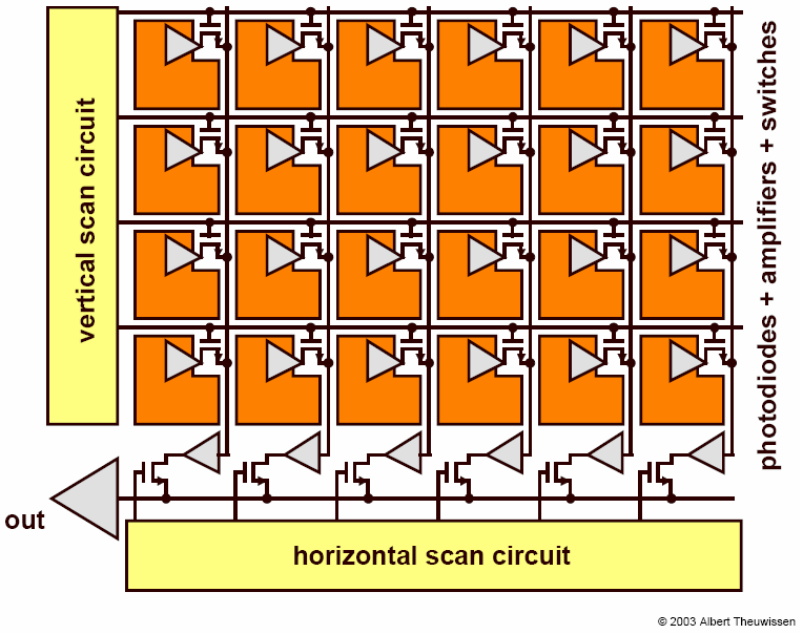
- Enhancement of the standard 3T APS
- Similar structure as in the APS

Each CMOS pixel based on:

- Along with pixels, an extra pinned photodiode is added and connected to the readout circuit by means of an extra transfer gate (TX).
- 4 transistors (Standard APS: 3 T)

Pros and cons :

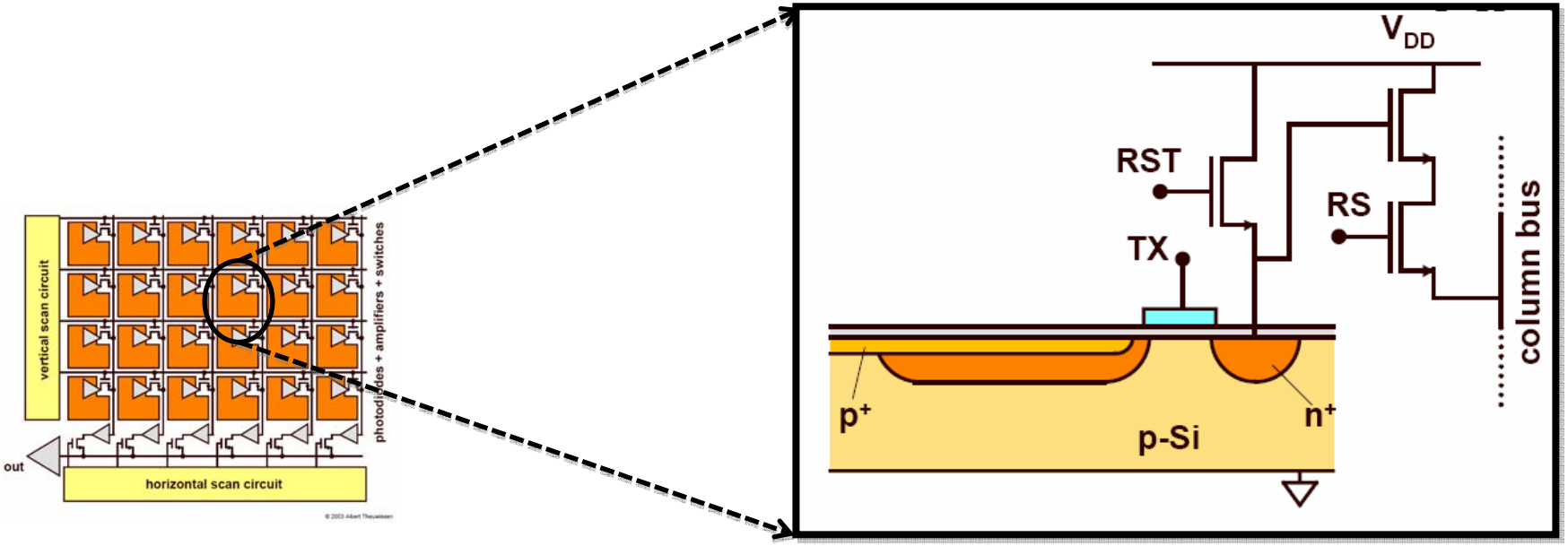
- Improvement of sensor readout speed and SNR,
- "Complicated" architecture results in a relatively low fill factor with pixels larger than 3 μ m



Various pixels

Working principle of the pinned photodiode APS

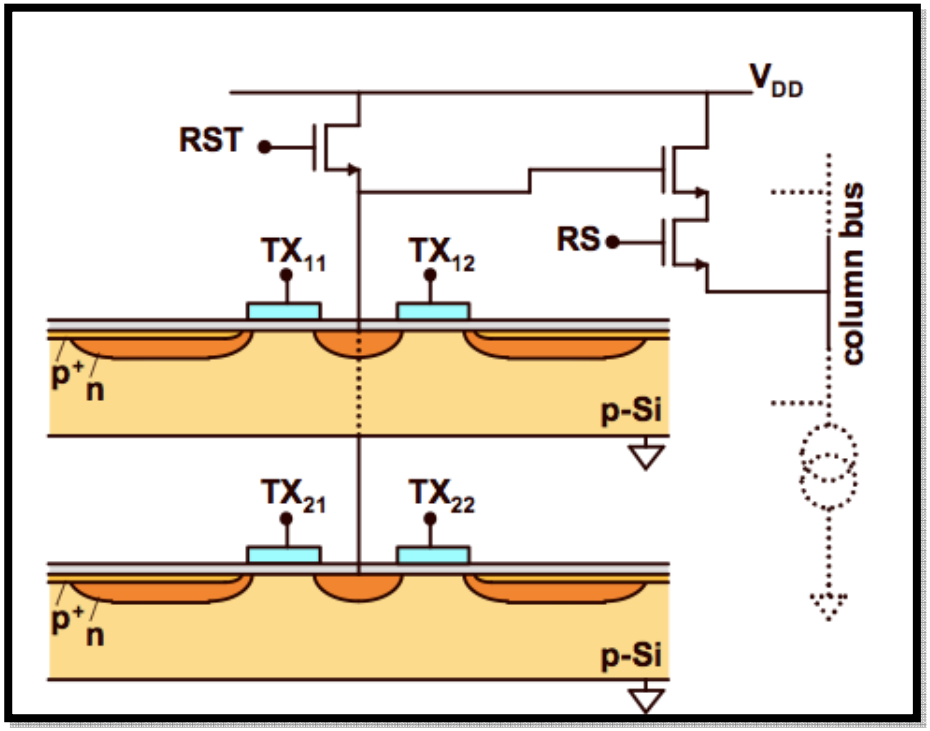
- Conversion of the photons is done in the (pinned) photodiode,
- At the end of the exposure, the readout node is reset by the reset transistor,
- A first measurement is the output voltage after reset,
- The photodiode is drained by activating TX and transferring all charges from the photodiode to the readout node,
- A second measurement is the output voltage after transfer,
- The two measurements are subtracted from each other (Correlated Double Sampling, CDS)



Various pixels

“Shared pixel” concept

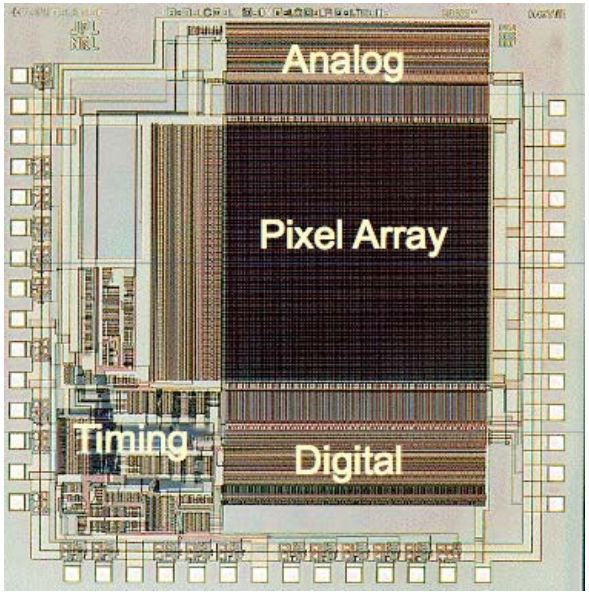
- **Several neighboring pixels share the same output circuitry,**
- **Ex: a group of 2 by 2 pixels have in common the source follower, the reset transistor, the addressing transistor and the readout node.**
- **Result: 1.75 T by pixel (8 T for 4 pixels)**
- **Pixel size down 1.45 μ m**

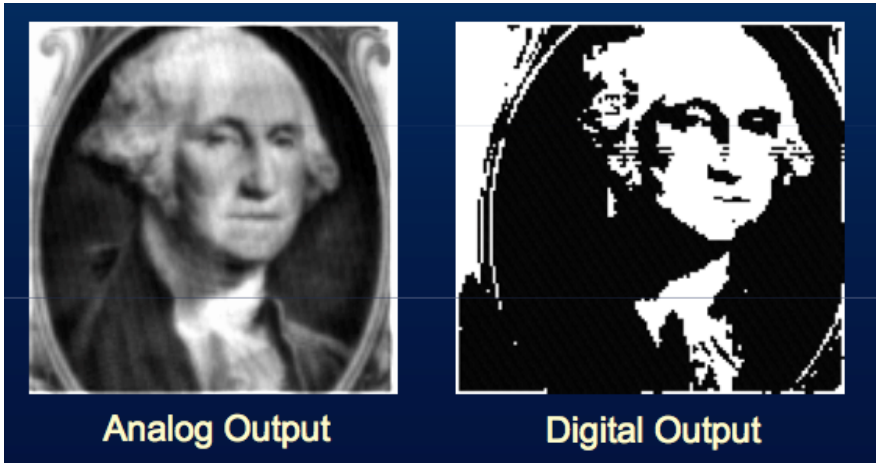


CMOS image sensors

On chip functionality

- On chip timing and control circuits
- On chip analog signal processing
  - Correlated double sampling
  - Fixed pattern noise suppression
  - Local neighborhood image processing
  - Pixel defect correction
- On chip analog to digital conversion
- On chip DSP and digital sensor control



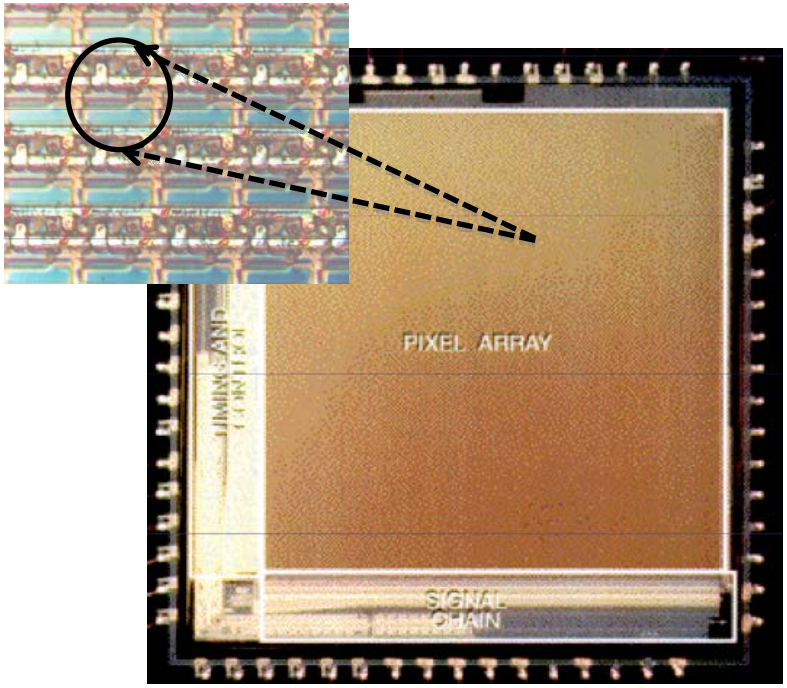


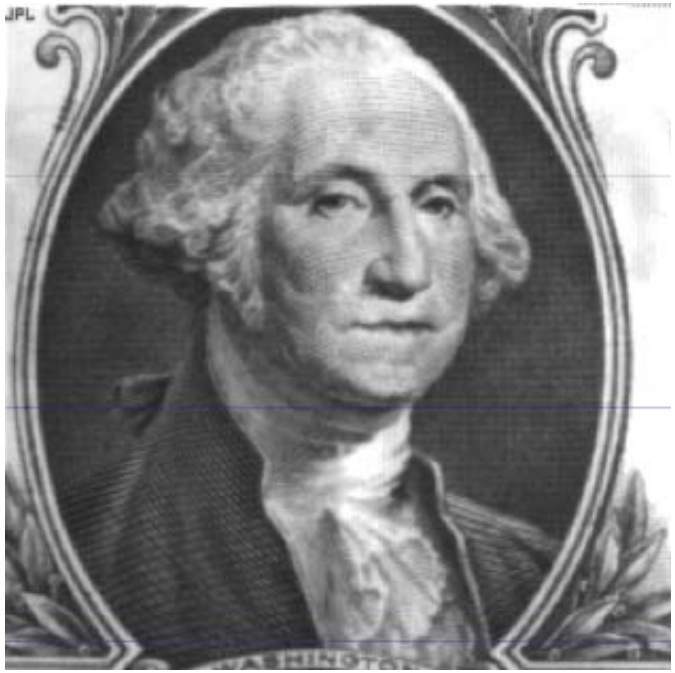
Famous analog imagers

First CMOS APS (1995) : E. Fossum (JPL Lab)

Nixon, R.H., et al., 256 ×256 CMOS Active Pixel Sensor Camera-on-a-Chip, IEEE Journal of Solid-State Circuits, vol. 31, No. 12, Dec. 1996, pp. 2046-2050

- **256 x 256 CMOS APS**
- **On chip Timing and control**
- **1.2um CMOS technology – pixel size: 20 um**



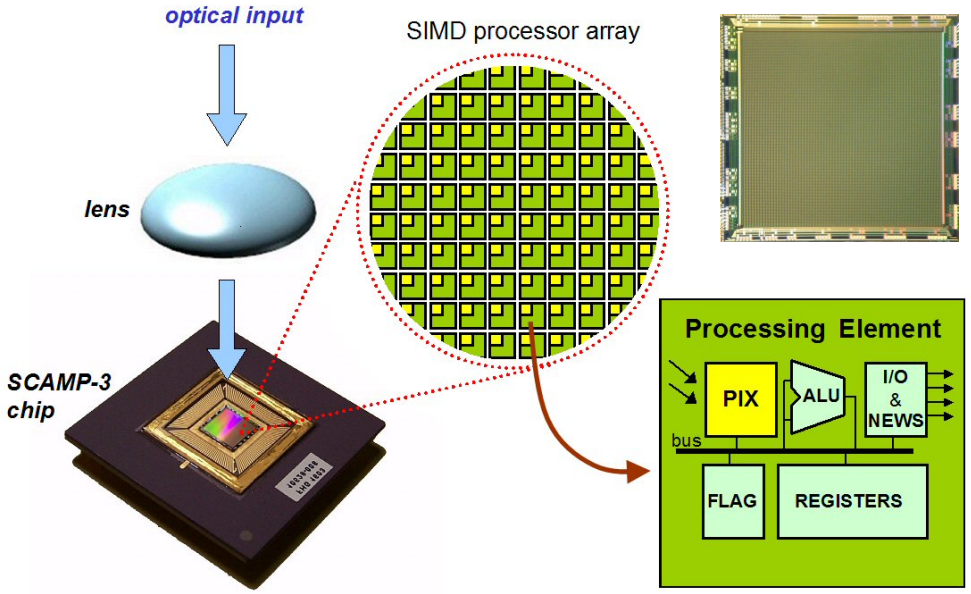


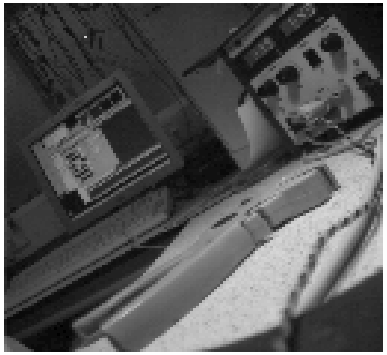
Famous analog imagers

SCAMP project: P. Dudek (The University of Manchester)

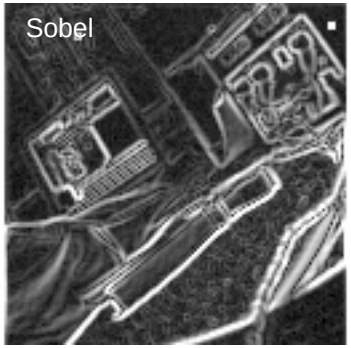
P.Dudek and S.J.Carey, "A General-Purpose 128x128 SIMD Processor Array with Integrated Image Sensor", Electronics Letters, vol.42, no.12, pp.678-679, June 2006

- **General-purpose programmable vision chip**
- **128x128 SIMD processor-per-pixel array fabricated**
- **0.35um CMOS technology**
- **PE size is about 50um x 50um**





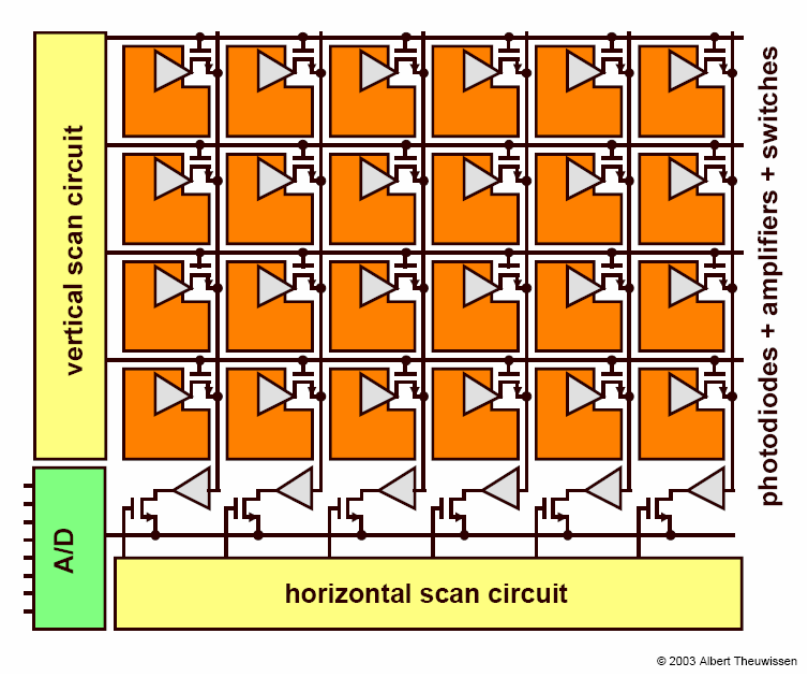
Motion detection

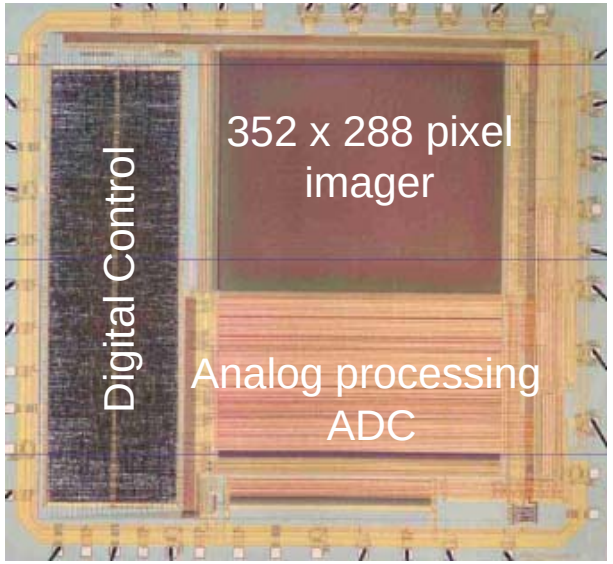


On-Chip A/D

Analog-to-digital Conversion (ADC)

- To convert the analog signal generated by the photodiodes into a digital signal, a single ADC can be added on chip
- With an on chip ADC, the maximum pixel frequency of the sensor can be limited when high accuracy is required (> 12 bits)
- This bottleneck is avoided by adding multiple ADCs (one per column, or even one per pixel)





Van Blerkom, Huang, Chan 1999

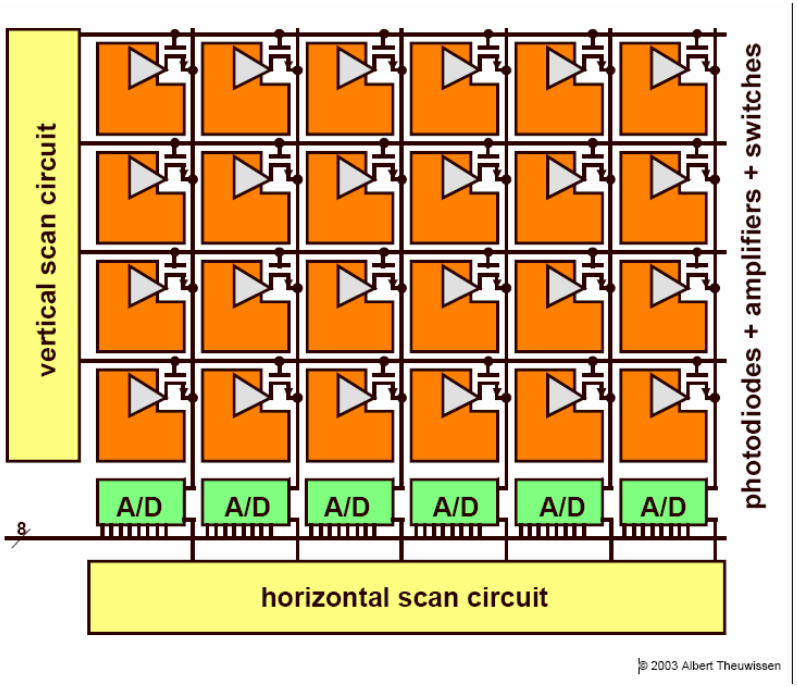
Column A/D

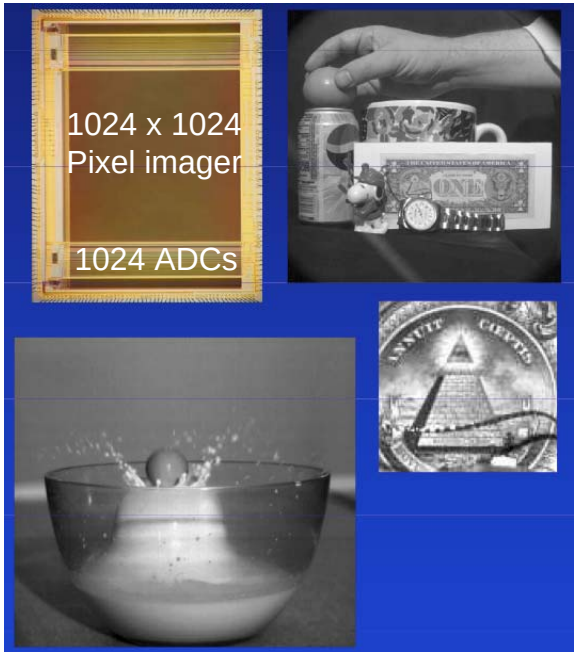
Column Analog-to-digital Conversion (ADC)

- The speed of each converter is descreased by the number of colums

Two main challenges:

- The space available for each ADC is limited to the horizontal pixel pitch
- The total area spent for the ADS becomes a significant part of the overall chip





Krymski, Van Blerkom, Bock, Anderson 1998

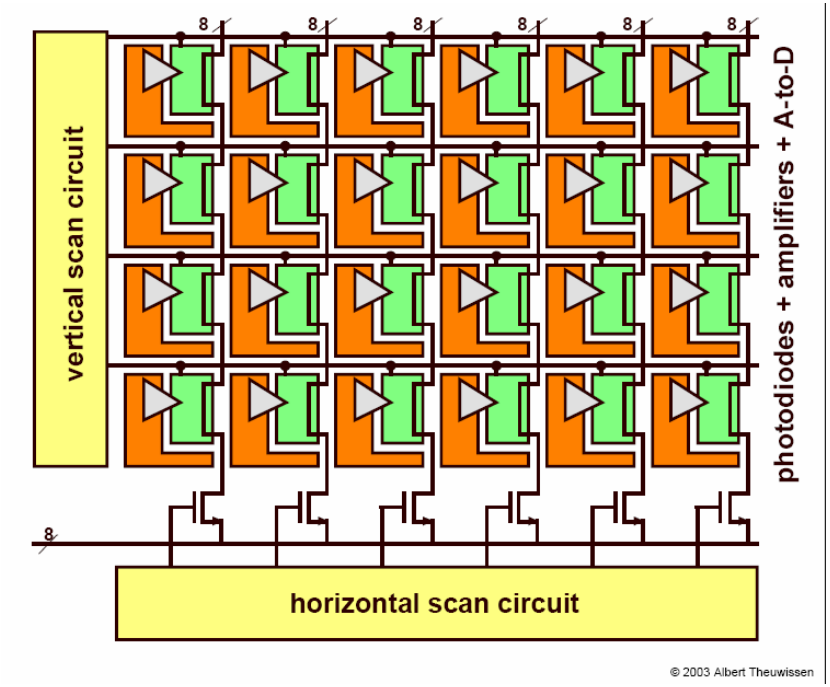
Pixel A/D

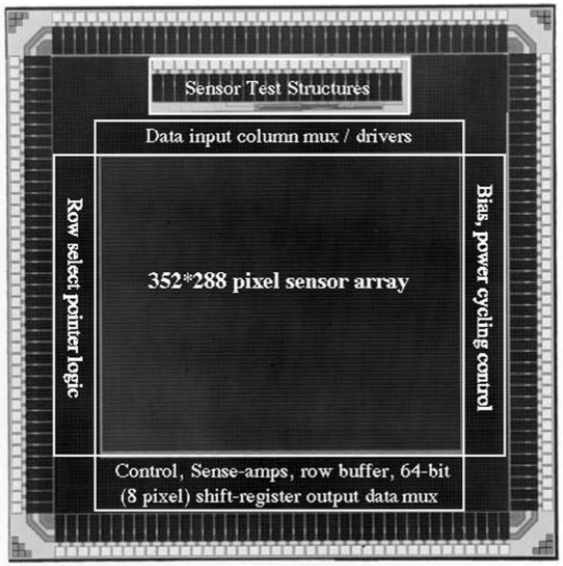
Pixel Analog-to-digital Conversion (ADC)

- Each pixel has its own ADC
- Resulting in Digital Pixel Sensor (DPS) architecture

Main challenges:

- ADC should be as compact as possible in order to keep a good fill factor
- A complete digital bus for each column must be routed (8 bits for example)





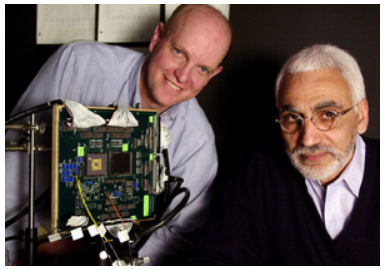
Kleinfelder et al, 2001

Famous digital imagers

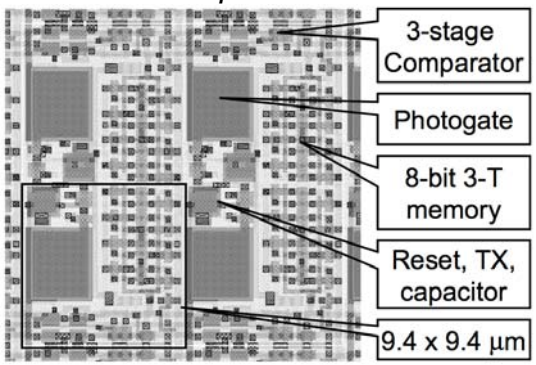
DPS project: El Gamal (Stanford University)

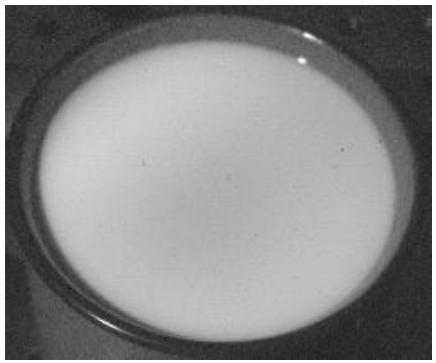
S. Kleinfelder, S. Lim, X. Liu, and A. El Gamal, "A 10 000 Frames/s CMOS Digital Pixel Sensor," IEEE Journal of Solid-State Circuits, vol. 36, no. 12, pp. 2049–2059, Dec 2001

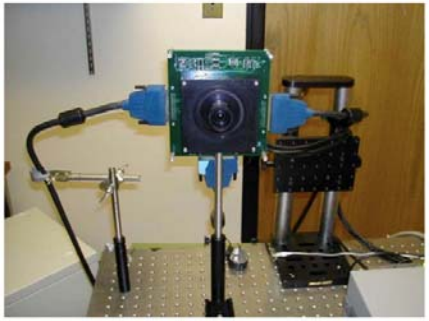
- **352x288 8-bit digital pixels with ADC and memory per pixel**
- **0.18um CMOS technology**
- **PE size is about 10um x 10um**
- **10 000 digital frames / sec**

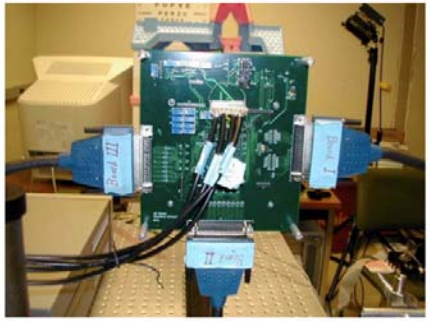


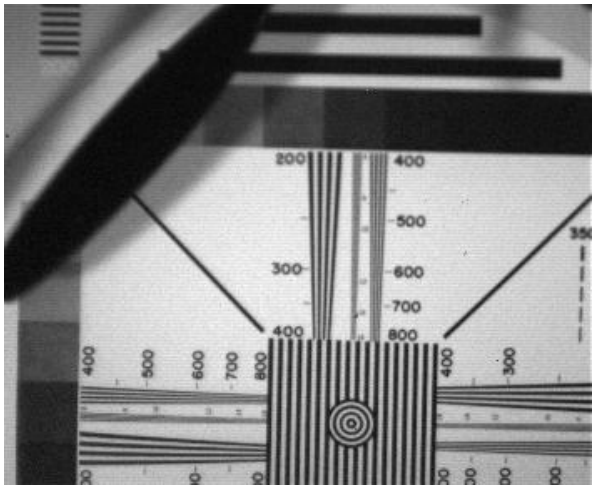
4 pixels











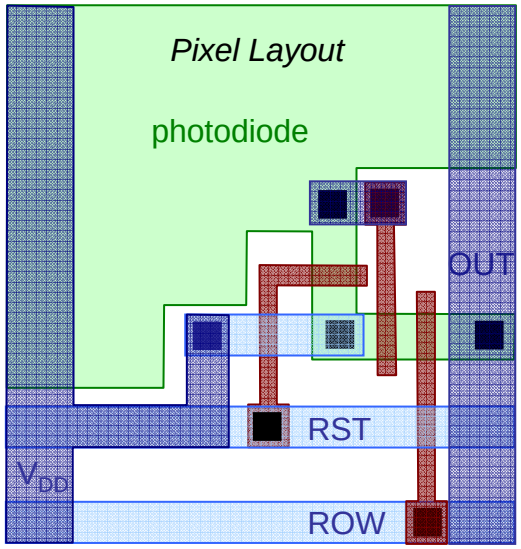
Limitations of Standard CMOS APS

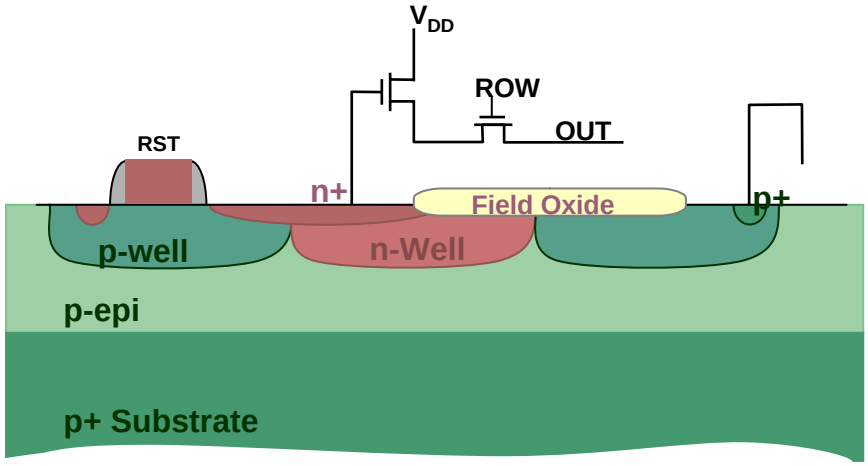
Fill factor tradeoff:

- **Photodetector and pixel transistors share same area**
- **Functionality limited by the size of pixels**

Challenge:

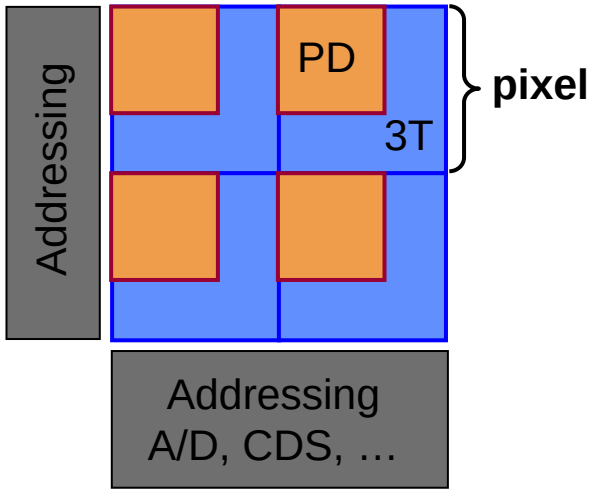
- **Increase the fill factor up to 100 % while integrating more complex processing elements using 3D integration**





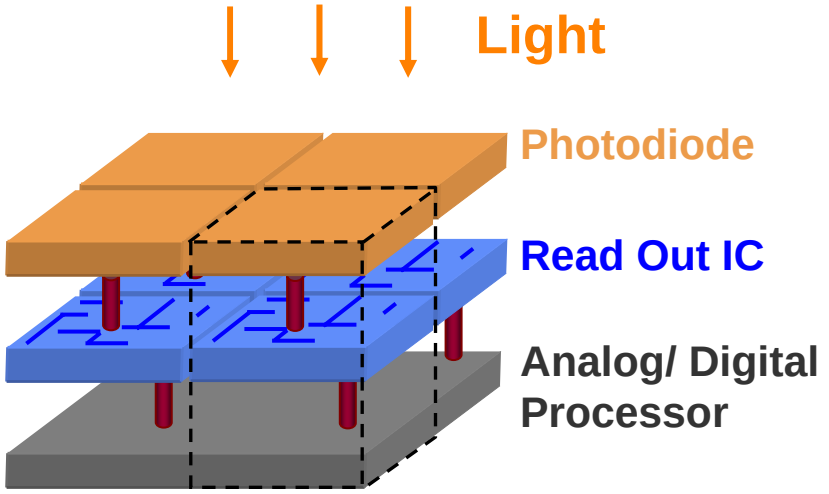
Advantages of Vertical Integration

Conventional Monolithic APS



- Pixel electronics and detectors share area
- Fill factor loss
- Co-optimized fabrication
- Control and support electronics placed outside of imaging area

3-D Pixel



- 100% fill factor detector
- Fabrication optimized by layer function
- Local image processing
  - Power and noise management
- Scalable to large-area focal planes